PCIE Bus Interface Chip CH368

Datasheet (I)

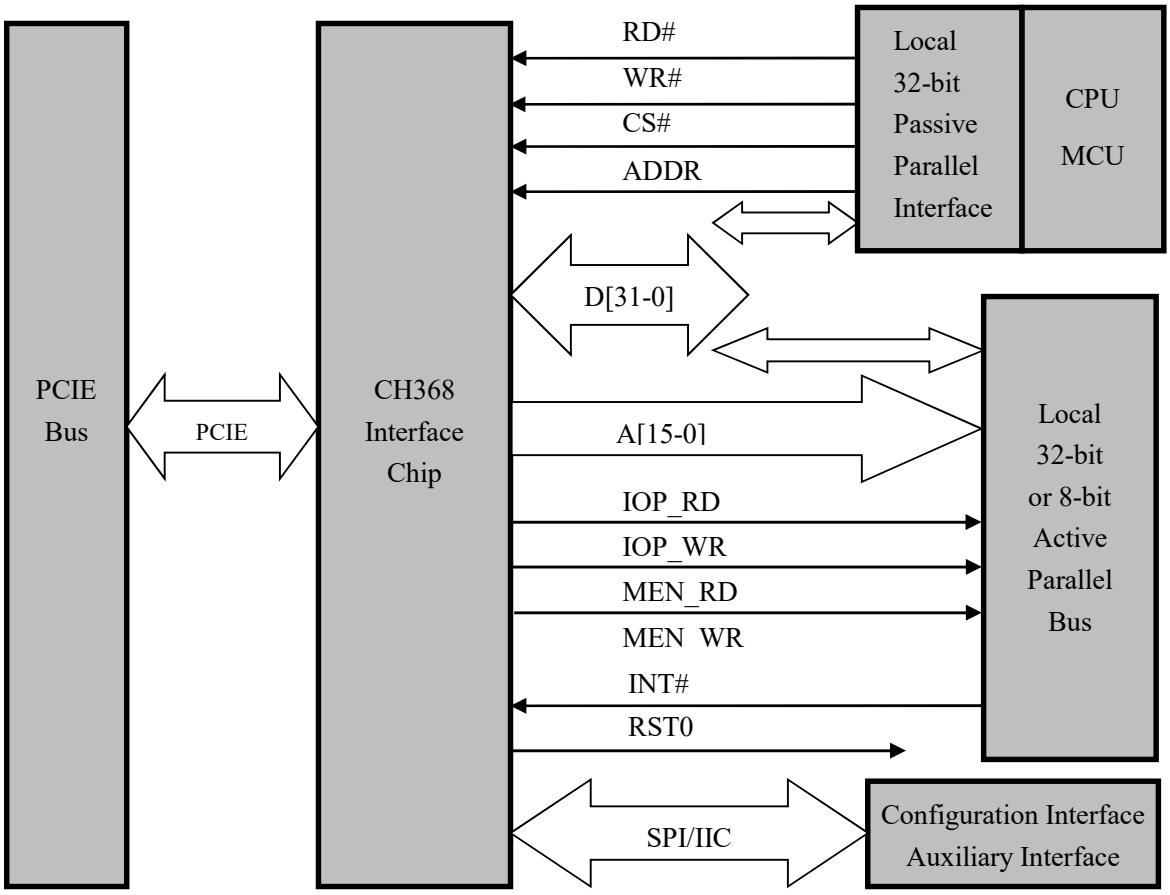
Version: 1B

https://wch-ic.com

1. Overview

CH368 is a general interface chip connected to the PCI-Express bus, supporting I/O port mapping, memory mapping, expansion ROM and interrupts. The CH368 converts the high-speed PCIE bus into an easy-to-use 32-bit or 8-bit active parallel interface similar to the ISA bus, which can be used to create low-cost PCIE-bus-based computer boards, as well as upgrading boards originally based on the ISA or PCI bus to the PCIE bus. Compared with other mainstream buses, PCIE bus is faster, more real-time and better controllable, so CH368 is suitable for high-speed real-time I/O control cards, communication interface cards, data acquisition cards and so on.

The figure below is its general application block diagram.

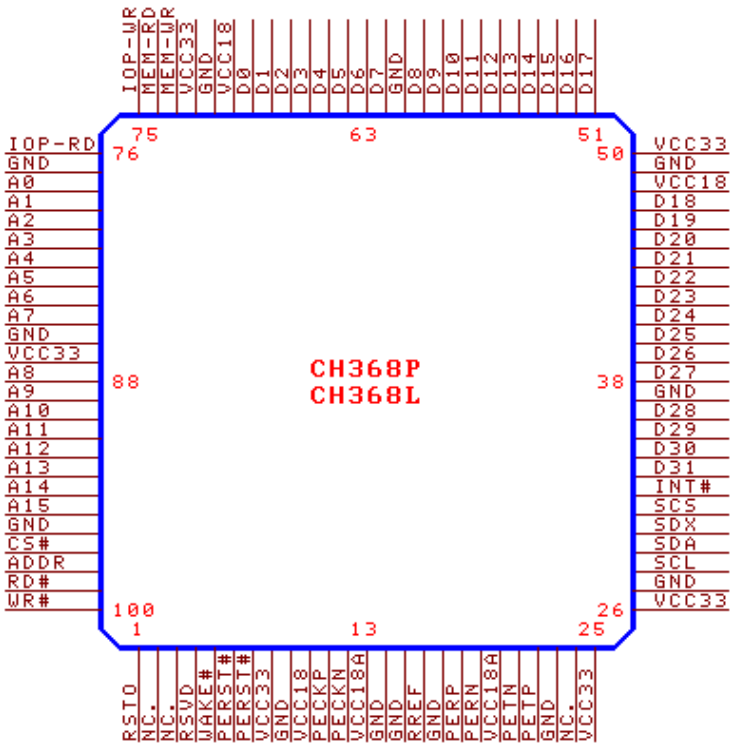


2. Feature

- Provide 8-bit or 32-bit active parallel bus based on PCIE bus.
- Provide a 32-bit passive parallel interface, can be connected to other CPUs or MCU buses.
- Support I/O reading and writing, automatically assign I/O base addresses, and support I/O ports up to 232 bytes in length.
- Support memory reading and writing and Memory prefetching, and direct mapping supports memory SRAM with a capacity of 32KB.

- The width of the read and write pulses is optional from 30nS to 450nS, and the 32-bit memory burst block access speed can reach 50MB per second.
- Support level interrupt or edge interrupt request input, and support interrupt sharing.
- Support flash expansion ROM booting without hard disk, and can provide subroutine library BRM for expansion ROM applications.
- Provide high-speed 3-wire or 4-wire SPI serial host interface.
- Provide a 2-wire serial host interface, which can be connected to a serial EEPROM device similar to 24C0X for storing non-volatile data.
- The device identification of PCIE board can be set in the EEPROM device (Vendor ID, Device ID, Class Code etc.)
- Built-in 2uS to 8mS hardware timing unit, used as a delay reference during software operation.
- Drive supports Windows 98/ME/NT4.0/2000/XP/Vista and Linux, and provides application layer API through the DLL.
- 3.3V power supply voltage, I/O pins support 5V tolerant voltage, and support low-power sleep mode.
- RoHS compliant and LQFP-100 lead-free package.

3. Package



Package Form	Shaping Width	Pin Spacing		Package Description	Order Model
LQFP100	14mm × 14mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH368P
LQFP100	14mm × 14mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH368L

Note: CH368P is externally powered at 3.3V and has a built-in 3.3V to 1.8V LDO step-down regulator, eliminating the need for an external supply of 1.8V;

CH368L requires external supply of both 3.3V and 1.8V.

4. Pin

4.1 Power Line

368P Pin No.	368L Pin No.	Pin Name	Type	Pin Description
8		VCC33	Power	3.3V I/O power supply and internal LDO buck supply inputs
	8	VCC33	Power	3.3V I/O power supply
25,26,50,72,87		VCC33	Power	3.3V I/O power supply
10		VCC18	Power	1.8V core power supply and internal LDO buck supply outputs
	10	VCC18	Power	1.8V core power
48,70		VCC18	Power	1.8V core power
13,20		VCC18A	Power	1.8V transmitting power
9,14,15,17,23,27,37, 49,61,71,77,86,96		GND	Power	Common ground
2,3,24		NC.	Empty pin	Forbidden to connect

4.2 PCIE Bus Signal Line

Pin No.	Pin Name	Type	Pin Description
6,7	PERST#	Input	System reset signal line, active low
11,12	PECKP/PECKN	Input	System reference clock differential input
18,19	PERP/PERN	PCIE input	PCIE receiver differential signal input
22,21	PETP/PETN	PCIE output	PCIE transmitter differential signal output
5	WAKE#	Open-drain	Bus wake-up output, active at low level, not connected if not used

4.3 Local Signal Line

Pin No.	Pin Name	Type	Pin Description
33-36 38-47 51-60 62-69	D31~D0	3-state output and input	32-bit bidirectional data signal line, built-in pull-up resistor
95-88 85-78	A15~A0	Output	16-bit address signal line, A15~A8 can be used as general output GPO to independently control the output
76	IOP_RD	Output	Read strobe of I/O port, low level pulse is active
75	IOP_WR	Output	Write strobe of I/O port, low level pulse is active
74	MEM_RD	Output	Memory read strobe, low level pulse is valid
73	MEM_WR	Output	Memory write strobe, low level pulse is valid
32	INT#	Input	Interrupt request input, level or edge valid, built-in pull-up resistor
99	RD#	Input	Read strobe of passive parallel interface, active low, built-in pull-up resistor
100	WR#	Input	Write strobe of passive parallel interface, active low, built-in pull-up resistor
97	CS#	Input	Chip select input of passive parallel interface, active low, built-in pull-up resistor
98	ADDR	Input	Passive parallel interface address input, SPI data input, built-in pull-up resistor

4.4 Auxiliary Signal Line

Pin No.	Pin Name	Type	Pin Description
16	RREF	Input	System reference current input, requires an external 12KΩ resistor to GND
28	SCL	Output	General-purpose output, SPI clock output, clock output of external configuration chip, can be externally connected to the SCL pin of the serial EEPROM configuration chip 24CXX
29	SDA	Open-drain output and input	General-purpose output and input, built-in pull-up resistor, must be high during reset, can be externally connected to the SDA pin of the serial EEPROM configuration chip 24CXX
30	SDX	3-state bidirectional	General-purpose output and input, SPI data output and input, built-in pull-up resistor
31	SCS	Output	General-purpose output, SPI chip selected output
1	RSTO	Output	Active low reset output, general-purpose output
4	RSVD	Reserved	Pins are reserved and connections are prohibited

5. Register

5.1 Power Line

5.1.1. Attribute abbreviation: R=completely read-only, W=readable and writable, S=read-only but can be set in advance, …=ellipsis.

5.1.2. Number system of data: If it ends with H, it is a hexadecimal number, otherwise it is a binary number.

5.1.3. Value wildcards and attributes: r=reserved (forbidden to use), x=any value, …=ellipsis.

5.2 PCIE Configuration Space

Address	Register Name	Register Properties	Default value after system reset
01H-00H	Vendor ID	SSSS	1C00H
03H-02H	Device ID	SSSS	5834H
05H-04H	Command	RRRRRWRWRWRRRWWW	0000000000000000
07H-06H	Status	RRRRRRRRRRRRRRR	000000000001x000
08H	Revision ID	SS	10H
0BH-09H	Class Code	SSSSSS	100000H
0FH-0CH		RRRRRRWW	00000000H
13H-10H	I/O Base Address	WWWWWWRR	00000001H
17H-14H	Memory Base Address	WWWWWWWWWWWWWWWW WRRRRRRRRRRRRRR	0000000000000000 0000000000001000
2BH-18H		RRRR….RRRR	0000….0000H
2DH-2CH	Subsystem Vendor ID	SSSS	Same as VID
2FH-2EH	Subsystem ID	SSSS	Same as DID
33H-30H	ROM Base Address	WWWWWWWWWWWWWWW WRRRRRRRRRRRRRW	0000000000000000 0000000000000000
3BH-34H		RRRR….RRRR	0000….0060H
3FH-3CH	Interrupt Line & Pin	RRRRRRRRRRRRRRR RRRRRRRRWWWWWWW	0000000000000000 0000000100000000
FFFH-40H	Reserved	(Disabled)	(Disabled)

5.3 I/O Base Address Register

The actual address of the register is the I/O base address plus the offset address in the table.

Offset address	Register Name	Abbreviation	Register properties	Default value after system reset
E7H-00H	Standard local I/O port	IOXR	WW	Connected to I/O device
E8H	General-purpose output register	GPOR	WWWRRWWW	000rr111
E9H	General-purpose variable register	GPVR	WWWWWWWW	00001010
EAH	General-purpose input register	GPIR	RRRRRRRR	11111rr1
EBH	Interrupt control register	INTCR	RRRWWWWW	rrr00000

EFH-ECH	Data registers for passive parallel interface	SLVDR	WWWWWWWW	xxxxxxxxH
F1H-F0H	A15-A0 address setting register	ADRSR	WWWW	8000H
F2H	Reserved		(Disabled)	xxH
F3H	Memory data access register	MEMDR	WW	Connected to memory
F7H-F4H	Data bus static input register	DBUSR	RRRRRRRR	xxxxxxxxH
F8H	Miscellaneous control and status registers	MICSR	WRRRRWRW	1rrr10r1
F9H	Reserved		(Disabled)	xxH
FAH	Read and write speed control register	SPDCR	RWWWWWWW	r0000111
FBH	Passive parallel interface control register	SLVCR	WRRRWWRR	000r0000
FCH	Hardware loop count register	CNTR	RR	xxH
FDH	SPI control register	SPICR	WWWRRRRR	0000xxxx
FEH	SPI data register	SPIDR	WW	xxH
FFH	Reserved		(Disabled)	xxH

5.4 Bit of Register

Register Name	Bit Address	Attributes	Bit usage instructions (Default value)	Bit value=0	Bit value =1
General-purpose output register GPOR (I/O base address+0E8H address)	Bit 0	W	Set output value of SDA pin (1)	Low	High
	Bit 1	W	Set output value of SCL pin (1)	Low	High
	Bit 2	W	Set output value of SCS pin (1)	Low	High
	Bit 5	W	Enable support for forced wake-up (0)	Not supported	Supported
	Bit 6	W	Set data direction of SDX pin (0)	Input	Output
	Bit 7	W	Set output value of SDX pin (0)	Low	High
General-purpose input register GPIR (I/O base address +0EAH address)	Bit 0	R	Input status of SDA pin (1)	Low	High
	Bit 3	R	Input status of INT# pin (1)	Low	High
	Bit 4	R	Input status of RD# pin (1)	Low	High
	Bit 5	R	Input status of WR# pin (1)	Low	High
	Bit 6	R	Input status of ADDR pin (1)	Low	High
	Bit 7	R	Input status of SDX pin (1)	Low	High
Interrupt control register INTCR (I/O base address +0EBH address)	Bit 0	W	MSI interrupt mode enable (0)	INTA interrupt	MSI interrupt
	Bit 1	W	Global interrupt enable (0)	Disable interrupt	Enable interrupt
	Bit 2	W	INT# pin interrupt input polarity (0)	Low level rising edge	High level falling edge
	Bit 3	W	INT# pin interrupt input type (0)	Level	Edge
	Bit 4	W	Interrupt request retry enable (0)	Disable retry	Enable retry

Miscellaneous control and status registers MICSR (I/O base address +0F8H address)	Bit 0	W	Set output value of A15 pin (1)	Low	High
	Bit 2	W	Interrupt activation status (0)	No interrupt	Interrupt
	Bit 3	R	Input status of INT# pin (1)	Low	High
	Bit 7	W	Set output value of RSTO pin (1)	Low	High
Speed control register SPDCR (I/O base address +0FAH address)	Bit 0 Bit 1 Bit 2 Bit 3	WWWW	The total width of the read and write signal (0111) including the setup time and hold time, the step size is 30nS, 0000~1111 corresponds to 60nS~510nS, the total width minus the setup time of bit 4, minus the hold time of bit 5, we get the read write pulse net width, minimum is 0nS, maximum is 480nS		
	Bit 4	W	Data and address output setup time (0)	15nS	45nS
	Bit 5	W	Data and address output hold times (0)	15nS	45nS
	Bit 6	W	Local data bus width (0)	8-bit	32-bit
Passive parallel interface control register SLVCR (I/O base address +0FBH address)	Bit 0 Bit 1	RR	Identification data from MCU (00)	Custom	
	Bit 2 Bit 3	WW	Identification data from PC to MCU (00)	Custom	
	Bit 4	R	Bus connection enable from MCU (0)	Not connected	Connect MCU
	Bit 6	R	Interrupt request from MCU (0)	No interrupt	Interrupt
	Bit 7	W	Interrupt request output from PC to MCU (0)	No interrupt	Interrupt
SPI control register SPICR (I/O base address +0FDH address)	Bit 0 ~Bit 3	RRRR	The upper 4 bits of the hardware cycle count (XXXX), combined with the hardware cycle count register CNTR, total 12 bits		
	Bit 4	R	SPI transfer in progress status (0)	Free	Transmitting
	Bit 5	W	Select SPI serial clock frequency (0)	31.3MHz	15.6MHz
	Bit 6	W	Select SPI data input pin (0)	SDX	ADDR
	Bit 7	W	Start a new transfer after enabling SPIDR reading (0)	Free after reading	Start after reading

6. Function Description

6.1 External Configuration Chip

The CH368 chip will check the data in the external 24CXX configuration chip every time it is powered on or the PCIE bus is reset. If the configuration chip is connected and the data is valid, it will be automatically loaded into the CH368 chip to replace the default PCIE identification information.

The configuration chip 24CXX is a 4-pin or 8-pin packaged non-volatile serial EEPROM memory. In addition to providing configuration information to CH368, it can also save some other parameters for the application program. CH368 supports the following models of 24CXX chips: 24C01 (A), 24C02, 24C04, 24C08, 24C16, etc.

The following table is the data definition in the configuration chip 24CXX.

Byte address	Abbreviation	Data usage description	Default value
00H	SIG	External configuration chip valid flag, must be 78H	78H
01H	CFG	Configuration parameters	00H
03H-02H	RSVD	(Reserved unit)	0000H
05H-04H	VID	Vendor ID	Custom
07H-06H	DID	Device ID	Custom
08H	RID	Revision ID	Custom
0BH-09H	CLS	Class Code	100000H
0DH-0CH	SVID	Subsystem Vendor ID	Custom
0FH-0EH	SID	Subsystem ID	Custom
1FH-10H	RSVD	(Reserved unit)	00H or FFH
Other address	APP	User or application custom unit	

6.2 Space Mapping

There are three types of spaces in a PC: Memory space, I/O space, and configuration space. The memory space mainly includes memory, video memory, expansion ROM, device buffer, etc. It is generally used to store large amounts of data and exchange data blocks. The I/O space mainly includes the control register and status register of the device, which are generally used to control and query the working status of the device and exchange a small amount of data. The configuration space is mainly used to provide the system with basic information about the device itself, and to accept the system's control and query of the global status of the device.

In order to avoid address conflicts, the PCIE bus requires that the addresses occupied by each device can be relocated. Relocation is implemented by the base address register of the device's configuration space. Normally, the base address register of each device is always assigned a different base address by the BIOS or operating system, thereby mapping each device to a different address range. Applications can also modify the base address themselves when needed.

The memory space of CH368 occupies 32K bytes, and the offset address is 0000H~7FFFH. It can all be provided to external devices. The actual address is the memory base address plus the offset address. The I/O space of CH368 occupies 256 bytes. If the CH368 self-use register is removed, 232 bytes can be provided for external devices to use. The offset address is 00H~E7H. The actual address is the I/O base address plus the offset address.

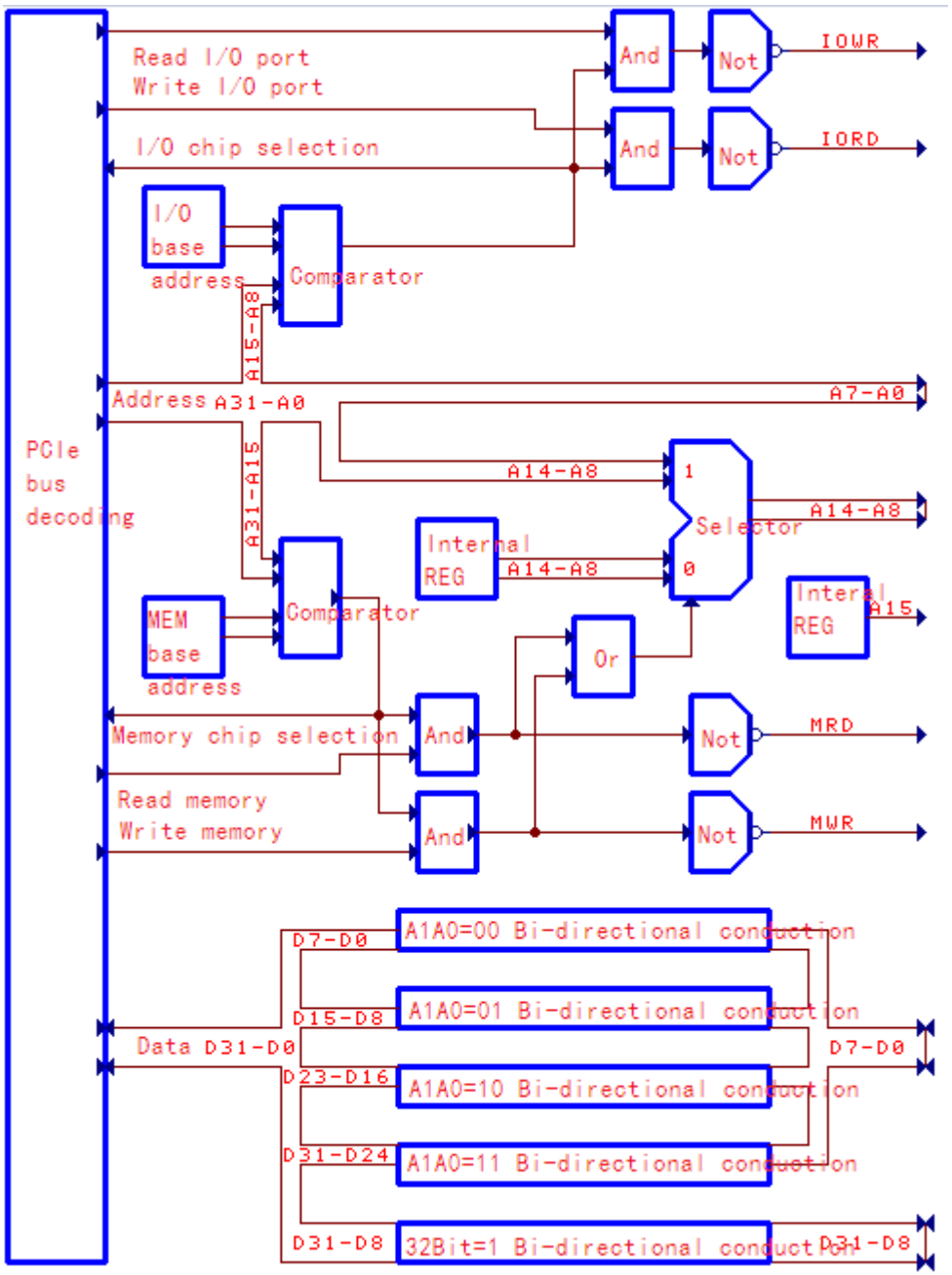
6.3 Active Bus Internal Structure and Signal Lines

The figure below is the main structure of the active parallel bus inside CH368. After CH368 decodes various signals on the PCIE bus, it generates internal data buses D31~D0, internal address buses A31~A0, read I/O port signals, write I/O port signals, read memory signals, write memory signals, etc. The transmission direction of each signal

has been marked in the figure.

The signals on the right side of the structure diagram refer to the various external pins provided by the CH368 to the local terminal. The address lines A15 to A0 are used to provide the offset address relative to the base address, and the data buses D31 to D0 are used for inputting data during read operations and outputting data during write operations. IOP_RD is used to provide the I/O read select pulse signal, IOP_WR is used to provide the I/O write select pulse signal, MEM_RD is used to provide the memory read select pulse signal, and MEM_WR is used to MEM_RD is used to provide the memory read select pulse signal, MEM_WR is used to provide the memory write select pulse signal, and the read/write select pulse signals of the above pins are all active low. the address lines, data bus, read/write select signals provided by CH368 are similar to those of the ISA bus, and therefore, it is very suitable for upgrading the ISA boards to the PCIE bus. And as can be seen from the figure, the read/write select signal provided by CH368 has been chip-selected and controlled inside the chip, and the read/write select signal outputted by CH368 is only valid within its base address mapping, so the external device no longer needs chip-select decoding. During I/O read and write operations, A7~A0 of CH368 output the offset address of the I/O port. The effective offset address range provided to external devices is 00H~E7H. The external device can further decode A7~A0. Generates a secondary chip select signal. During the I/O read and write operations, A15~A8 of CH368 remain unchanged, but can be set to high level or low level in advance by the internal register.

During memory read and write operations, A14~A0 of CH368 output the offset address of the memory, and the effective offset address range provided to external devices is 0000H~7FFFH. During memory read and write operations, A15 of CH368 remains unchanged, but can be set to high level or low level in advance by the internal register for memory address line expansion or page selection.



6.4 Data Width

CH368 supports the PC program to read and write the I/O port or memory in single-byte units. When the local data bus width (bit 6 of the read-write speed control register SPDCR) is set to 1, CH368 supports the PC program to read and write in four-byte units. Read-write I/O ports or memories in units of bytes (double words). The internal registers of CH368 (located at the I/O base address +0E8H and above) always support PC program access in single-byte, double-byte (word), and 4-byte (double-word) units.

When performing a double-byte access, the starting address must be the address of any word boundary within the base address range (a multiple of 2); when performing a 4-byte access, the starting address must be any double word within the base address range. The address of the boundary (a multiple of 4).

6.5 Read and Write Memory via I/O

In general, the local memory of the CH368 is mapped to the memory space of the computer, and reading and writing

the local memory is carried out in the memory space. In order to facilitate the operation of addressing under BIOS or DOS, the CH368 also provides a method of shifting the memory space to the I/O space, which is applicable to the memory with more orderly data access. This method directly supports 64KB capacity memory, independent of the memory 4GB space and memory base address. The steps for reading and writing memory space via I/O are shown in the following table.

Register	Register operations	Read data program (ASM)	Read data program (C/C++)

A15~A0 address setting register ADRSR	Write starting address	mov dx, PORT_ADDR
		mov ax, START_ADDR
		out dx, ax
			outport (PORT_ADDR,
			START_ADDR);

Memory data access register MEMDR	Read and write data sequentially Address automatically added	mov dx, PORT_DATA
		mov di, BUFFER_ADDR
		mov cx, LENGTH
		rep insb
			int i;
			char buf[LENGTH];
			for (i=0; i<LENGTH; ++i)
			buf[i]=inportb(PORT_DATA);

Constants and variables used in the program:

PORT_ADDR represents the port address of the A15-A0 address setting register (i.e.: I/O base address + 0F0H);

PORT_DATA represents the port address of the memory data access register (i.e.: I/O base address + 0F3H);

START_ADDR represents the starting address of the data to be accessed in the memory;

LENGTH represents the length of the data to be accessed, that is, the number of bytes;

BUFFER_ADDR represents the starting address of the buffer that stores the read data; buf is the data buffer.

6.6 Hardware Interrupt

CH368 supports level or edge interrupt request input, which is selected by bit 3 of the interrupt control register INTCR. Its polarity is selected by bit 2. There are four types: active low level, active high level, active rising edge, active falling edge.

In the edge interrupt mode, when a valid edge input is detected on the INT# pin, the CH368's interrupt activation status bit (bit 2 of the Miscellaneous Control and Status Register MICSR) is automatically set to 1 to memorize the edge and request an interrupt from the PCIE bus. After entering the interrupt service program, software must clear this interrupt activation status bit in time to cancel (end) this interrupt request.

In the level interrupt mode, when the INT# pin detects a valid level input, CH368 directly applies for an interrupt to the PCIE bus. When the input level is invalid, CH368 will cancel (end) this interrupt request to the PCIE bus. If the interrupt request is canceled soon after CH368 applies for an interrupt to the PCIE bus, then this interrupt request may be ignored by the PC.

If the PC program sets the interrupt activation status bit of CH368 to 1 in software, it can also make CH368 enter the interrupt activation status and apply for an interrupt from the PCIE bus. Such software interrupt has exactly the same characteristics as the hardware interrupt caused by the external input of the INT# pin, and can be used to test the interrupt function of CH368.

The standard interrupt process is as follows:

① The external circuit outputs a valid interrupt request signal to the INT# pin.

② CH368 applies for an interrupt from the PC through the PCIE bus (for edge interrupts, the interrupt activation status bit needs to be memorized first).

③ The PC enters the interrupt service program of CH368.

④ The interrupt service routine performs necessary interrupt processing. This step can also be executed before exiting the interrupt.

⑤ If it is a level interrupt, the interrupt service program should notify the external circuit to cancel the interrupt request.
⑥ If it is an edge interrupt, the interrupt service routine must clear the interrupt activation status bit to 0.
⑦ CH368 cancels the interrupt request to the PC through the PCIE bus.
⑧ After the interrupt processing is completed, the PC exits the interrupt service program of CH368.

6.7 Example Description

Design a PCIE board similar to the printing port based on CH368. The design agrees that the I/O offset address 00H of the board is the data port, the offset address 01H is the status port, and the offset address 02H is the control port. When inserted into a PC, the board may be assigned an I/O base address of 9500H, then the actual I/O address of the data port is 9500H, the I/O address of the status port is 9501H, and the I/O address of the control port is 9502H. Distinguishing each port is achieved by performing address decoding on A7~A0 of CH368. If other ports are not needed, only A1~A0 can be simplified and decoded.

If two identical boards of the above-mentioned cards are inserted into the PC, the second board will also be automatically assigned an I/O base address by the system, but it will certainly not be the same as the I/O base address of the first board. If the I/O base address of the second board is C700H, the actual I/O address of the control port of the second board is C702H, thus making the two identical PCIE boards have different I/O port addresses respectively, and avoiding I/O address conflicts.

Board designers and related applications know the offset address of each port in advance, but cannot know the I/O base address of the board in advance. Therefore, the application needs to pass the board before performing I/O operations on the PCIE board. The I/O base address register of the configuration space understands the I/O base address of the current board, and then calculates the actual I/O address of each port based on the I/O base address plus the offset address of each port. The I/O address performs I/O operations on each port.

The memory aspect is similar to the I/O port. Take CH368 connected to a 32KB capacity dual-port SRAM for high-speed data exchange as an example. If the memory base address of CH368 is allocated as E3050000H, then the computer program reads and writes the physical address range E3050000H~E3057FFFH to read and write the dual-port SRAM. Note that actual PC programs usually use converted virtual addresses rather than physical addresses; in addition, if you want to read and write memory under DOS, you may need to use a system environment that supports the 4GB address range.

Below is an example of the corresponding read and write processes.

① Write data 5AH to the control port, corresponding to the C language program "outportb (IoBase+2,0x5A)", where the variable IoBase is equal to the actual base address 0x9500 automatically assigned by the system. After execution, the address lines A7~A0 of CH368 output the offset address 02H of the control port (the address 9502 is decomposed into the base address 9500H and the offset address 02H, CH368 only outputs the offset address, not the base address), and the data line D7 of CH368 ~D0 outputs 5AH, and IOP_WR outputs a low-level pulse. The pulse width is preset by the read and write speed control register of CH368, and the default is 240nS.
② Reading data from the data port and status port corresponds to the C language program "inport(IoBase+0)". The low byte of the returned result is the data read from the data port, and the high byte is the data read from the status port. After execution, the address lines A7~A0 of CH368 first output the offset address 00H of the data port, and at the same time IOP_RD outputs the first low level pulse. The external device should output the data to the data bus D7~D0; then the address lines A7 of CH368 ~A0 outputs the offset address of the status port 01H, and at the same time IOP_RD outputs the second low level pulse. The external device should output the status to the data bus D7~D0.
③ Memory reading and writing are similar to I/O reading and writing, but there are two differences: first, the

address lines A14~A0 of CH368 output 15-bit offset addresses, while I/O only outputs 8-bit offset addresses from A7~A0; The second is to use the MEM_RD pin to output the read control signal instead of the IOP_RD pin to output the read control signal, and use the MEM_WR pin to output the write control signal instead of the IOP_WR pin to output the write control signal, so that external devices can distinguish memory read and write operations. It is not a read or write operation of the I/O port.

The I/O port of CH368 has the same data transfer speed as the memory, except that the instructions of the PC in the I/O space are less than those in the memory space. In general, external devices can map register units such as control and status to I/O space, and map data block exchange buffers to memory space.

6.8 Other Application Description

The RSTO pin of the CH368 chip is a reset output and is active at low level. During the system reset, the RSTO pin outputs a low level; after completing the loading of the SPI interface FlashROM configuration information, the RSTO outputs a high level; then the IIC interface EEPROM configuration information is loaded; Finally, the CH368 chip enters the normal working state, the RSTO pin switch to general-purpose output pin.

CH368 provides a 32-bit data bus static input register DBUSR. When reading this register, the read and write strobe control lines of I/O and memory will not output signals, so the static values of the current local data bus D31~D0 can be read. Similar to a GPI general-purpose input pin. If a pull-down resistor is connected to the D6 pin of the data bus, bit 6 of the read data is 0, otherwise it is 1.

The CH368 provides a hardware timing unit (SPICR[3:0]+CNTR) with a width of 12 bits, taking the 204.8 division frequency of the PCIE bus main frequency as the timing input. For the standard 100MHz main frequency of the PCIE bus, the hardware loop counter register increases one count every 2.048uS, and it takes 8388.608uS for the count from 000H to 0FFFH and then loop to 000H. By comparing the difference between the counts read before and after, the actual delay time can be calculated and used to replace the computer software instruction loop with large error.

The output pins of CH368 are all 3.3V LVCMOS level, compatible with 5V TTL level, and the input pins, except PCIE signal pin, RD# pin, WR# pin and CS# pin, are all able to tolerant 5V voltage, compatible with 5V CMOS level, 3.3V LVCMOS and 5V TTL and LVTTL level.

7. Parameters

7.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	CH368P	-40	85	℃
		CH368L	-40	85	℃
TS	Ambient temperature during storage		-55	125	℃
VCC33	I/O power voltage (VCC33 to power, GND)		-0.4	4.2	V
VCC18 VCC18A	Core power voltage (VCC18 to power, GND) Transmission supply voltage (VCC18A to power, GND)		-0.4	2.3	V
VIO	Voltage on PCIE signals and RD#/WR#/CS# input or output pins		-0.4	VCC33+0.4	V
VIO5	Voltage on other input or output pins		-0.4	5.4V	V

7.2 Electrical Parameters (Test conditions: TA=25℃, VCC=5V, does not include pins to connect to USB bus)

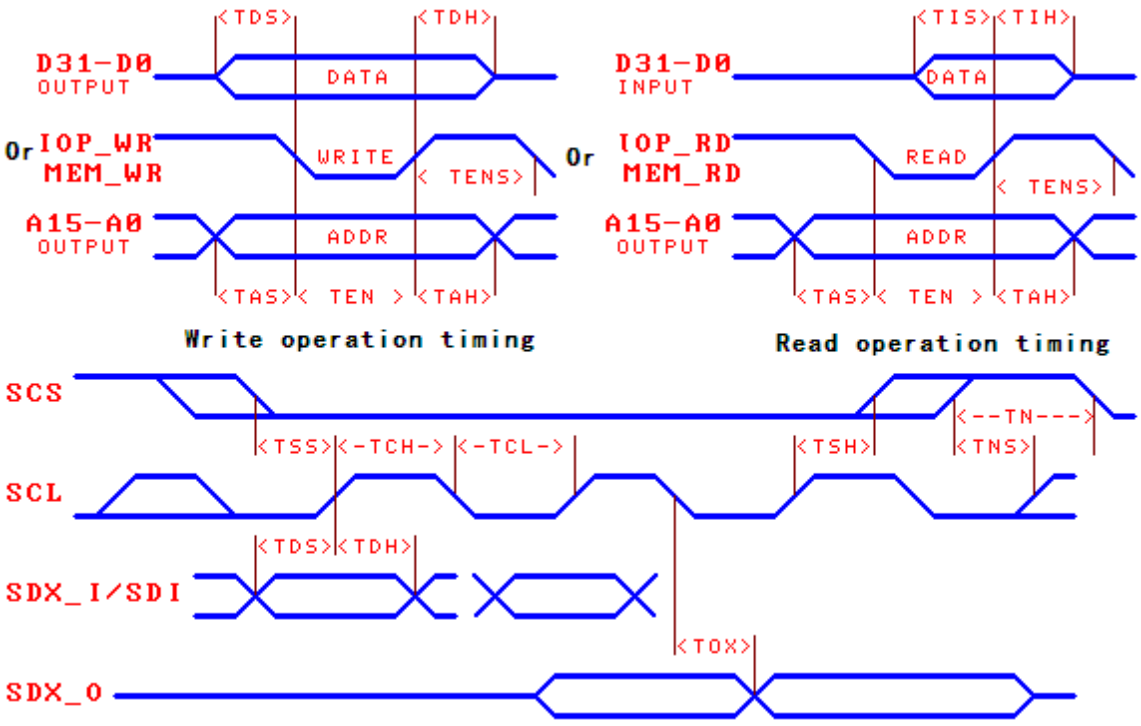
Name	Parameter description	Min.	Typ.	Max.	Unit
VCC33	I/O power voltage	3.0	3.3	3.6	V
VCC18 VCC18A	Core power voltage Transmission supply voltage	1.65	1.8	1.95	V
ICC	Total supply current during operation		230	300	mA
VIL	low level input voltage	-0.4		0.7	V
VIH	High level input voltage	2.0		VCC33+0.4	V
VOL6	A11~A0 Low level output voltage (6mA sink current)			0.4	V
VOL8	IOP_RD、IOP_WR、MEM_RD、 MEM_WR、RSTO、 A15~A12 Low level output voltage (8mA sink current)			0.4	V
VOL	Other pins low level output voltage (4mA sink current)			0.4	V
VOH	High level output voltage (4mA output current)	VCC33-0.4			V
IIN	Input current without pull-up input			10	uA
IUP	Input current with pull-up input	20	40	100	uA

7.3 Timing Parameters (Test conditions: TA=25℃, VCC33=3.3V, refer to figure blew)

Name	Parameter description	Min.	Typ.	Max.	Unit
FCLK	CLK input frequency (Main frequency of the PCIE bus)	0	100	105	MHz
FSCL2	SCL output frequency when the 2-wire interface is automatically loaded		244	260	KHz

FSCL3	SCL output frequency when 3-wire interface is automatically loaded		31	35	MHz
TINTEG	Minimum pulse width for active edge interrupt	5			nS
TEN	IOP_RD, IOP_WR, MEM_RD, MEM_WR Read strobe or write strobe low pulse width	30	Optional 30~480	480	nS
TENS	IOP_RD、IOP_WR、MEM_RD、MEM_WR Continuous strobe high level interval width	60			nS
TAS	Address A15~A0 output establishment time	12	Optional 15 or 45		nS
TAH	Address A15~A0 output holding time	12	Optional 15 or 45		nS
TDS	Data D31~D0 output setup time	12	Optional 15 or 45		nS
TDH	Data D31～D0 output holding time	12	Optional 15 or 45		nS
TIS	Data D31～D0 input establishment time	10			nS
TIH	Data D31～D0 input holding time	0			nS
TSS	SCS valid setup time before SCK rising edge	11	16 or 32		nS
TSH	SCS valid hold time after SCK rising edge	11	16 or 32		nS
TNS	SCS invalid setup time before SCK rising edge	10			nS
TN	SCS invalid time (SPI operation interval time)	110			nS
TCH	SCK clock high level time	13	16 or 32		nS
TCL	SCK clock low level time	13	16 or 32		nS
TDS	Input establishment time of SDX/SDI before SCK rising edge	5			nS
TDH	Input holding time of SDX/SDI before SCK rising edge	0			nS
TOX	SCK falling edge to SDX output valid or changed	0	2	5	nS
TSRD	Read strobe pulse width of passive parallel interface	35			nS
TSWR	Write strobe pulse width of passive parallel interface	35			nS
TSSP	The interval between operations of passive parallel interface	45			nS
TSDS	Data output valid time of passive parallel interface	2	5	12	nS
TSDH	Data output hold time of passive parallel interface		8	16	nS
TSAS	Address input setup time of passive parallel interface	5			nS
TSAH	Address input hold time of passive parallel interface	3			nS

TSIS	Data input setup time of passive parallel interface	5			nS
TSIH	Data input hold time of passive parallel interface	3			nS



8. Application

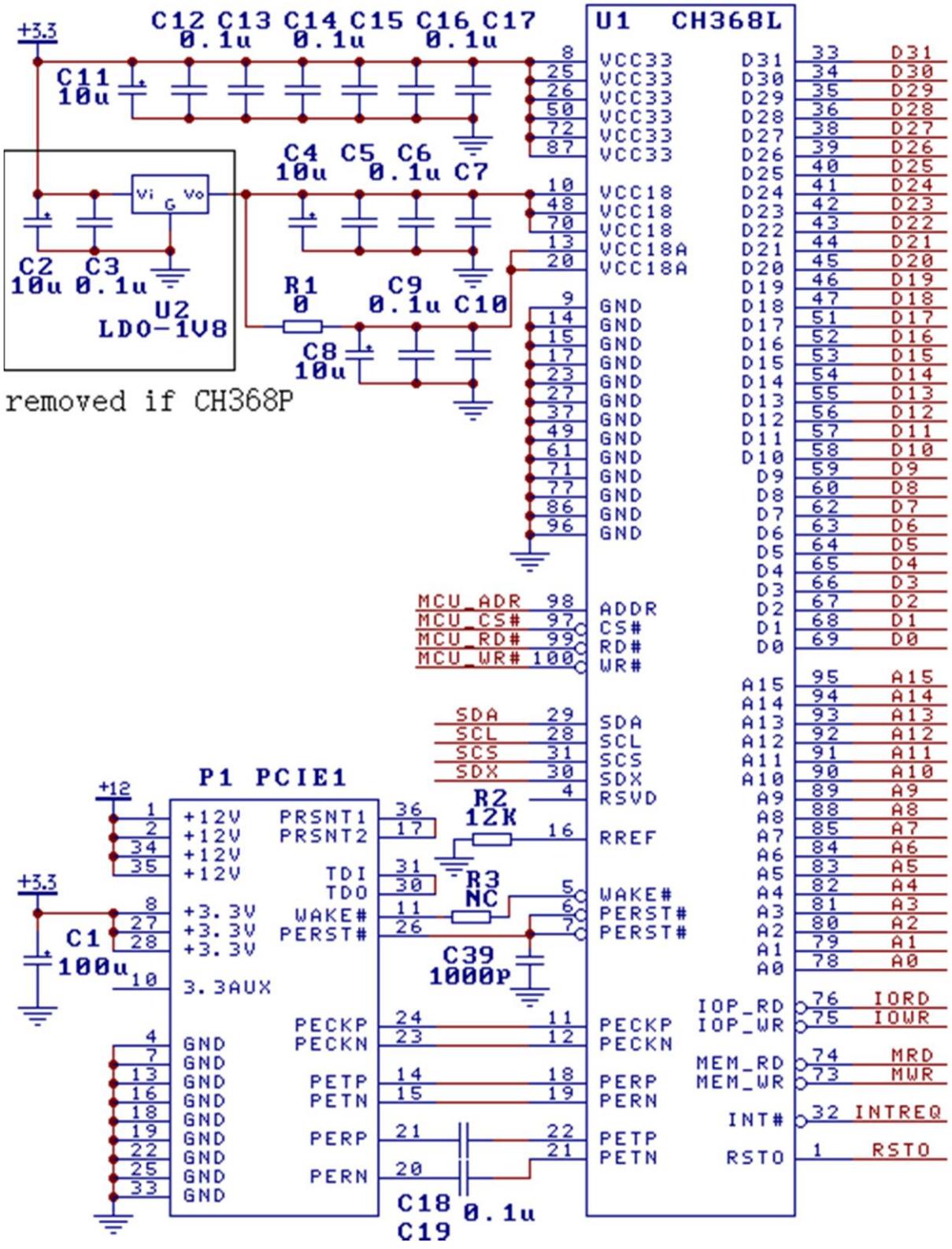
8.1. Connect to PCIE Bus

This is the basic circuit for connecting the CH368 chip to the PCIE bus.

Capacitor C39 in the figure is used for power-on reset, and other capacitors are used for power supply decoupling. The capacitor with a capacity of 10uF is an MLCC or tantalum capacitor, and the capacitor with a capacity of 0.1uF is a high-frequency capacitor. They are connected in parallel to the power pins of CH368.

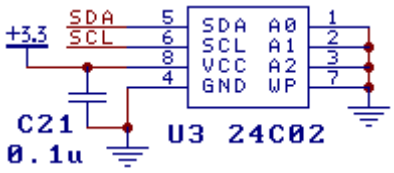
Any unused pins can be left unconnected.

CH368 belongs to high-frequency circuits, please refer to the PCIE bus specification when designing the PCB board, or refer to the PCIE_PCB.PDF.



8.2. Connect to Configuration Chip (Figure blew)

The CH368 supports the external EEPROM configuration chip 24CXX, which is used to provide identification information of PCIE boards such as VID/DID.



8.3. Connect to MCU

There are four methods for bidirectional data transmission between PC and MCU or DSP through CH368: First, use dual-port SRAM, so that CH368 and MCU can read and write the same memory, and perform bidirectional data exchange in large data blocks; Second, use the bidirectional buffer interface chip CH421, which provides a 64-byte buffer for the CH368 to write to the MCU and the MCU to write to the CH368, respectively, and conducts bidirectional data exchange in 64-byte data blocks. Third, use the passive parallel interface of CH368 (D31~D0, RD#, WR#, CS#, ADDR) to provide asynchronous data exchange, bidirectional data exchange in units of 32-bit data, without adding additional hardware costs; Fourth, the SPI host interface of CH368 is used in bytes. No additional hardware costs are required for data exchange.