8-bit enhanced USB MCU CH552, CH551

Datasheet

Version: 1E

http://wch.cn

1. Overview

CH552 is an enhanced E8051 core MCU compatible with MCS51 instruction set. 79% of its instructions are single-byte single-cycle instructions, and the average instruction speed is 8 ~ 15 times faster than that of the standard MCS51.

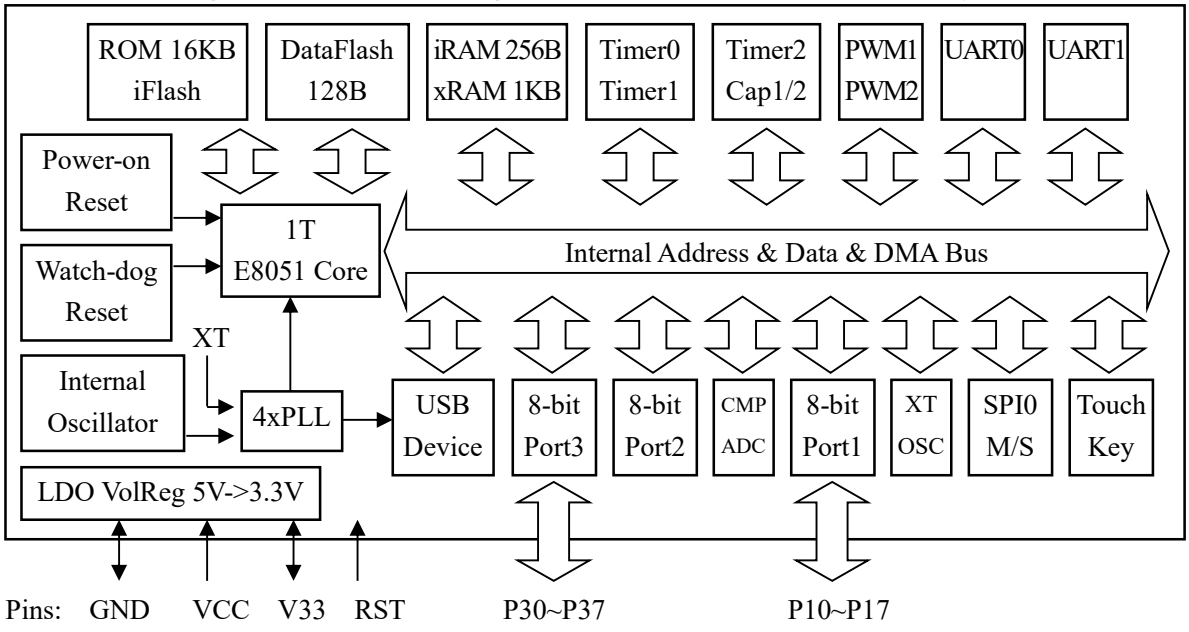
CH552 supports the maximum 24MHz system dominant frequency, with built-in 16K program memory ROM and 256-byte internal iRAM and 1K-byte internal xRAM. xRAM supports DMA direct memory access.

CH552 has built-in ADC analog-digital conversion, touch key capacitance detection, 3 sets of timers and signal capture and PWM, double UARTs, SPI, USB device controller and full-speed transceiver and other functional modules.

CH551 is a simplified version of CH552. The program memory ROM is 10K, the on-chip xRAM is 512 bytes, the asynchronous serial port is only UART0, the package form is only SOP16, the touch key only has 4 channels, and ADC analog-digital conversion module and USB type-C module are removed, and others are the same as those of CH552. Please directly refer to CH552 datasheet and materials.

Model	Program ROM	RAM	DataFlash	USB device	type-C	Timer	PWM	UART	SPI	ADC	Touch key
CH552	16KB	1280	128	Full/low speed	Configurable	3 sets	2 sets	2 sets	Master/slave	4 channels	6 channels
CH551	10KB	768			None			1 set		None	4 channels

The following is the internal block diagram of CH552 which is for reference only.

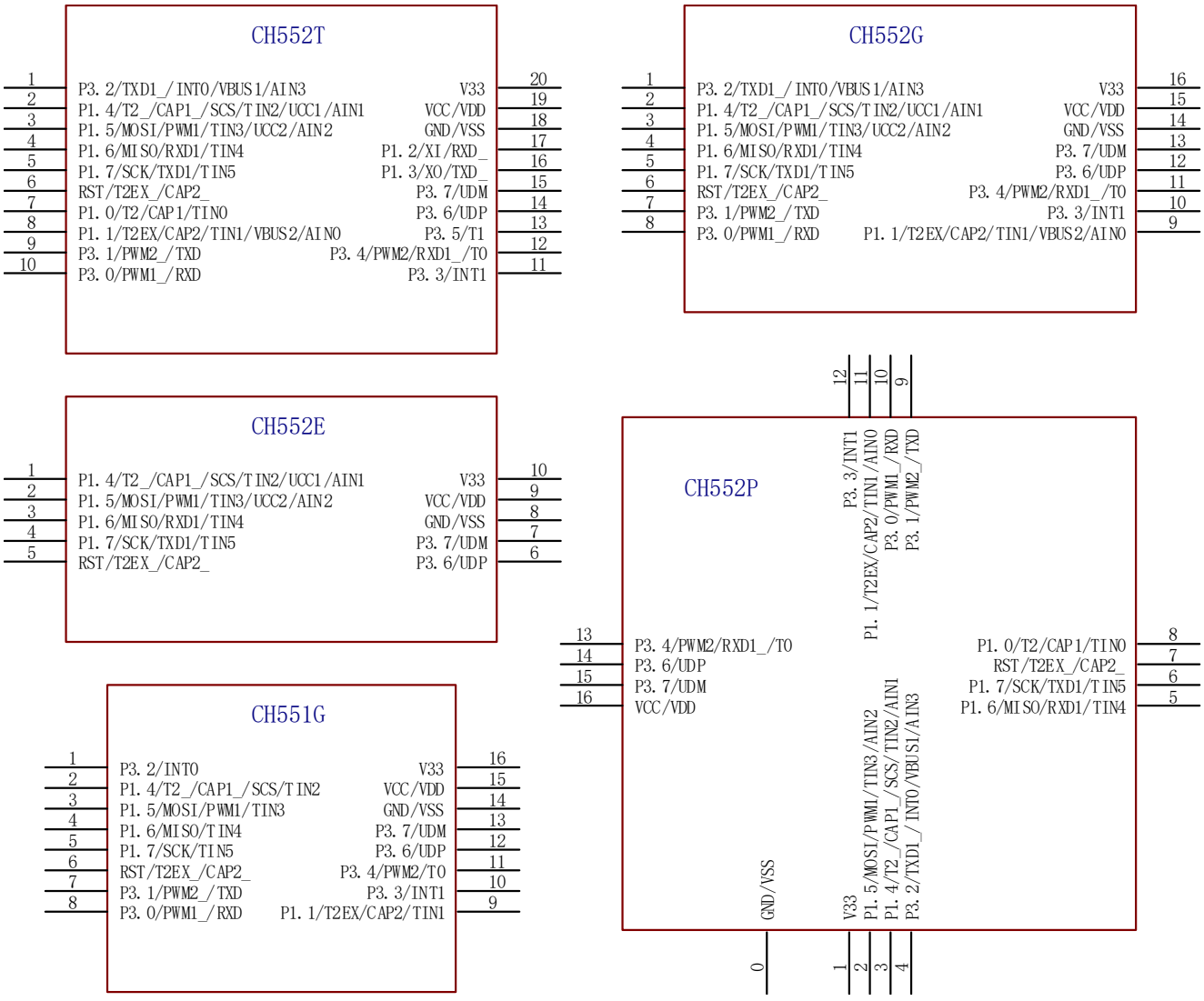


2. Features

- Core: Enhanced E8051 core compatible with MCS51 command set, 79% of its commands are single-byte single-cycle commands, and the average command speed is 8 ~ 15 times faster than that of the standard MCS51, with special XRAM data fast copy command, and double DPTR pointer.
- ROM: Non-volatile memory ROM that can be programmed for many times, with the capacity of 16KB, can all be used for program storage. Or it can be divided into a 14KB program storage area and a 2KB BootLoader/ISP program area.
- DataFlash: 128-byte non-volatile data memory that can be erased for multiple times and supports rewrite data in unit of byte.
- RAM: 256-byte internal iRAM, which can be used for fast temporary storage of data and stack. 1KB on-chip xRAM, which can be used for temporary storage of large amount of data and DMA direct memory access.
- USB: Built-in USB controller and USB transceiver, support USB-Device mode, support USB type-C master-slave detection, support USB 2.0 full speed 12Mbps or low speed 1.5Mbps. Support data packet of up to 64 bytes, built-in FIFO, and support DMA.
- Timer: 3 sets of timers, T0/T1/T2 is the standard MCS51 timer.
- Capture: Timer T2 is extended to support 2-channel signal capture.
- PWM: 2 sets of PWM output, PWM1/PWM2 is 2-channel 8-bit PWM output.
- UART: 2 sets of UARTs. Both support higher communication baud rate. UART0 is a standard MCS51 serial port.
- SPI: The SPI controller has built-in FIFO, and the clock frequency can reach half of the system dominant frequency Fsys. It supports simplex multiplex of serial data input and output, and Master/Slave mode.
- ADC: 4-channel 8-bit A/D converter. It supports voltage comparison.
- Touch-key: 6-channel capacitance detection. It supports up to 15 touchkeys, and supports independent timing interrupt.
- GPIO: It supports up to 17 GPIO pins (including XI/XO and RST as well as USB signal pins).
- Interrupt: It supports 14 sets of interrupt signal sources, including 6 sets of interrupts compatible with the standard MCS51 (INT0, T0, INT1, T1, UART0, T2), and 8 sets of extended interrupts (SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG). And GPIO interrupt can be selected from 7 pins.
- Watch-Dog: 8-bit presettable watchdog timer WDOG, support timing interrupt.
- Reset: It supports 4 kinds of reset signal sources, built-in power on reset, supports software reset, watchdog overflow reset and optional pin external input reset.
- Clock: Built-in 24MHz clock source, which can support external crystals by multiplexing GPIO pins.
- Power: Built-in 5V to 3.3V low dropout voltage regulator. It supports 5V or 3.3V or even 2.8V supply voltage. Support low-power sleep mode and external wake-up of USB, UART0, UART1, SPI0 and part of GPIOs.
- Unique built-in ID number of chip.

3. Package

Package	Width of Plastic		Pitch of Pin		Instruction of Package	Ordering Information
TSSOP-20	4.40mm	173mil	0.65mm	25mil	Small and thin 20-pin patch	CH552T
SOP-16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin patch	CH552G
QFN-16	3*3mm		0.50mm	19.7mil	Square leadless 16-pin	CH552P
MSOP-10	3.0mm	118mil	0.50mm	19.7mil	Miniature 16-pin patch	CH552E
SOP-16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin patch	CH551G



4. Pins

Pin No.			Pin Name	Other function names (Left function priority)	Other function description
TSSOP20	SOP16	QFN16			
19	15	16	VCC	VDD	Power input, requires an external 0.1uF power decoupling capacitor.
20	16	1	V33		Internal USB power regulator output and internal

					USB power input, When supply voltage is less than 3.6V, connect with VCC to input external power supply. When supply voltage is greater than 3.6V, connect with an external 0.1uF power decoupling capacitor.
18	14	0 bottom PAD	GND	VSS	Common ground.
6	6	7	RST	RST/T2EX_/CAP2_	The pin with underscore suffix is a mapping of the homonymous pin with no underscore. RST pin built-in pull-down resistor. Other GPIO have pull-up resistor in default. RST: External reset input. T2: External count input/clock output of Timer/Counter 2. T2EX: Reload/capture input of Timer/Counter 2. CAP1, CAP2: Capture input 1, 2 of Timer/Counter 2. TIN0 ~ TIN5: Touch key capacitance detection input of channel 0# ~ 5#. AIN0 ~ AIN3: ADC analog signal input of channel 0# ~ 3#. UCC1, UCC2: USB type-C bidirectional configuration channel. VBUS1, VBUS2: USB type-C bus voltage detection input. XI, XO: External crystal oscillation input, inverted input. RXD, TXD: UART0 serial data input, serial data output. SCS, MOSI, MISO, SCK: SPI0 interface, SCS is chip selection input, MOSI is host output/slave input, MISO is host input/slave output, SCK is serial clock. PWM1, PWM2: PWM1 output, PWM2 output. RXD1, TXD1: UART1 serial data input, serial data output. INT0, INT1: External interrupt 0, external interrupt 1 input. T0, T1: Timer 0, Timer 1 external input. UDM and UDP: D- and D+ signal terminals of USB device. Note: P3.6 and P3.7 internally use V33 as I/O power, so the high level of the input and output can only reach the voltage V33, and 5V is not supported
7	-	8	P1.0	T2/CAP1/TIN0	
8	9	11	P1.1	T2EX/CAP2/TIN1 /VBUS2/AIN0	
17	-	-	P1.2	XI/RXD_	
16	-	-	P1.3	XO/TXD_	
2	2	3	P1.4	T2_/CAP1_/SCS /TIN2/UCC1/AIN1	
3	3	2	P1.5	MOSI/PWM1/TIN3 /UCC2/AIN2	
4	4	5	P1.6	MISO/RXD1/TIN4	
5	5	6	P1.7	SCK/TXD1/TIN5	
10	8	10	P3.0	PWM1_/RXD	
9	7	9	P3.1	PWM2_/TXD	
1	1	4	P3.2	TXD1_/INT0 /VBUS1/AIN3	
11	10	12	P3.3	INT1	
12	11	13	P3.4	PWM2/RXD1_/T0	
13	-	-	P3.5	T1	
14	12	14	P3.6	UDP	
15	13	15	P3.7	UDM	

5. Special Function Register SFR

The following abbreviations may be used in this datasheet to describe the registers:

Abbreviation	Description
RO	Read only
WO	Write only, the read value is invalid
RW	Readable and writable
H	End with it to indicate a hexadecimal number
B	End with it to indicate a binary number

5.1 SFR Introduction and Address Distribution

CH552 controls and manages the device, and sets the working mode with a special function register SFR.

SFR occupies 80H-FFH address range of the internal data storage space and can only be accessed by direct address commands. Registers with the address x0h or x8h are addressable by bit to avoid modifying the values of other bits when accessing a specific bit. Other registers with the addresses that are not the multiple of 8 can only be accessed by bytes.

Some SFRs can be written only in safe mode, while they can be read only in non-safe mode, for example: GLOBAL_CFG, CLOCK_CFG, WAKE_CTRL.

Some SFRs have one or more aliases, for example: SPI0_CK_SE/SPI0_S_PRE.

Some addresses correspond to multiple independent SFRs, for example: SAFE_MOD/CHIP_ID, ROM_CTRL/ROM_STATUS.

CH552 contains the 8051 standard SFR register, and other device control registers are added. See the table below for the specific SFR.

Table 5.1 Special Function Register Table

SFR	0, 8	1, 9	2, A	3, B	4, C	5, D	6, E	7, F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP		RESET_KEEP	WDOG_COUNT
0xF0	B							
0xE8	IE_EX	IP_EX	UEP4_1_MOD	UEP2_3_MOD	UEP0_DMA_L	UEP0_DMA_H	UEP1_DMA_L	UEP1_DMA_H
0xE0	ACC	USB_INT_EN	USB_CTRL	USB_DEV_AD	UEP2_DMA_L	UEP2_DMA_H	UEP3_DMA_L	UEP3_DMA_H
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_RX_LEN	UEP0_CTRL	UEP0_T_LEN	UEP4_CTRL	UEP4_T_LEN
0xD0	PSW	UDEV_CTRL	UEP1_CTRL	UEP1_T_LEN	UEP2_CTRL	UEP2_T_LEN	UEP3_CTRL	UEP3_T_LEN
0xC8	T2CON	T2MOD	RCAP2L	RCAP2L	TL2	TH2	T2CAP1L	T2CAP1H
0xC0	SCON1	SBUF1	SBAUD1	TKEY_CTRL	TKEY_DATL	TKEY_DATH	PIN_FUNC	GPIO_IE
0xB8	IP	CLOCK_CFG						
0xB0	P3	GLOBAL_CFG						
0xA8	IE	WAKE_CTRL						
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX					
0x98	SCON	SBUF	ADC_CFG	PWM_DATA2	PWM_DATA1	PWM_CTRL	PWM_CK_SE	ADC_DATA
0x90	P1	USB_C_CTRL	P1_MOD_OC	P1_DIR_PU			P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_L	ROM_DATA_H

0x80	ADC_CTRL	SP	DPL	DPH	ROM_ADDR_L	ROM_ADDR_H	ROM_CTRL ROM_STATUS	PCON

Notes :(1) Those with red text can be addressed by bit; (2) The following shows the corresponding description of the color box

	Register address
	SPI0 related register
	ADC related register
	Touch-Key related registers
	USB related register
	Timer/counter 2 related register
	Port setting related register
	PWM1 and PWM2 related registers
	UART1 related register
	Flash-ROM related register

5.2 SFR Classification and Reset Value

Table 5.2 SFR Description and Reset Value

Function Classification	Name	Address	Description	Reset value
System setting related registers	B	F0h	B register	0000 0000b
	ACC	E0h	Accumulator	0000 0000b
	PSW	D0h	Program state register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (in CH552 Bootloader state)	1010 0000b
			Global configuration register (in CH552 application program state)	1000 0000b
			Global configuration register (in CH551 Bootloader state)	1110 0000b
			Global configuration register (in CH551 application program state)	1100 0000b
	CHIP_ID	A1h	ID code of CH552 (read only)	0101 0010b
			ID code of CH551 (read only)	0101 0001b
	SAFE_MOD	A1h	Safe mode control register (write only)	0000 0000b
	DPH	83h	The higher 8 bits of data address pointer	0000 0000b
	DPL	82h	The lower 8 bits of data address pointer	0000 0000b
	DPTR	82h	DPL and DPH constitute a 16-bit SFR	0000h
	SP	81h	Stack pointer	0000 0111b
Clock, sleep and power supply control related	WDOG_COUNT	FFh	Watchdog count register	0000 0000b
	RESET_KEEP	FEh	Reset hold register (in power on reset state)	0000 0000b
	CLOCK_CFG	B9h	System clock configuration register	1000 0011b
	WAKE_CTRL	A9h	Sleep wake-up control register	0000 0000b
	PCON	87h	Power control register (in power on reset state)	0001 0000b

registers				
Interrupt control related registers	IP_EX	E9h	Extend interrupt priority control register	0000 0000b
	IE_EX	E8h	Extend interrupt enable register	0000 0000b
	GPIO_IE	C7h	GPIO interrupt enable register	0000 0000b
	IP	B8h	Interrupt priority control register	0000 0000b
	IE	A8h	Interrupt enable register	0000 0000b
Flash-ROM related registers	ROM_DATA_H	8Fh	Flash-ROM data register high byte	xxxx xxxxb
	ROM_DATA_L	8Eh	Flash-ROM data register low byte	xxxx xxxxb
	ROM_DATA	8Eh	ROM_DATA_L and ROM_DATA_H constitute a 16-bit SFR	xxxxh
	ROM_STATUS	86h	flash-ROM state register (read only)	0000 0000b
	ROM_CTRL	86h	flash-ROM control register (read only)	0000 0000b
	ROM_ADDR_H	85h	flash-ROM address register high byte	xxxx xxxxb
	ROM_ADDR_L	84h	flash-ROM address register low byte	xxxx xxxxb
	ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitute a 16-bit SFR	xxxxh
Port setting related registers	PIN_FUNC	C6h	Pin function selection register	1000 0000b
	XBUS_AUX	A2h	External bus auxiliary setting register	0000 0000b
	P3_DIR_PU	97h	P3 port direction control and pull-up enable register	1111 1111b
	P3_MOD_OC	96h	P3 port output mode register	1111 1111b
	P1_DIR_PU	93h	P1 port direction control and pull-up enable register	1111 1111b
	P1_MOD_OC	92h	P1 port output mode register	1111 1111b
	P3	B0h	P3 port input and output register	1111 1111b
	P2	A0h	P2 port output register	1111 1111b
	P1	90h	P1 port input and output register	1111 1111b
Timer/counter 0 and 1 related registers	TH1	8Dh	Timer 1 count high byte	xxxx xxxxb
	TH0	8Ch	Timer 0 count high byte	xxxx xxxxb
	TL1	8Bh	Timer 1 count low byte	xxxx xxxxb
	TL0	8Ah	Timer 0 count low byte	xxxx xxxxb
	TMOD	89h	Timer0/1 mode register	0000 0000b
	TCON	88h	Timer0/1 control register	0000 0000b
UART0 related registers	SBUF	99h	UART0 data register	xxxx xxxxb
	SCON	98h	UART0 control register	0000 0000b
Timer/counter 2 related registers	T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	xxxx xxxxb
	T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxxx xxxxb
	T2CAP1	CEh	T2CAP1L and T2CAP1H constitute a 16-bit SFR	xxxxh
	TH2	CDh	Timer 2 counter high byte	0000 0000b

	TL2	CCh	Timer 2 counter low byte	0000 0000b
	T2COUNT	CCh	TL2 and TH2 constitute a 16-bit SFR	0000h
	RCAP2H	CBh	Count reload/capature 2 data register high byte	0000 0000b
	RCAP2L	CAh	Count reload/capature 2 data register low byte	0000 0000b
	RCAP2	CAh	RCAP2L and RCAP2H constitute a 16-bit SFR	0000h
	T2MOD	C9h	Timer2 mode register	0000 0000b
	T2CON	C8h	Timer2 control register	0000 0000b
PWM1 and PWM2 related registers	PWM_CK_SE	9Eh	PWM clock frequency division setting register	0000 0000b
	PWM_CTRL	9Dh	PWM control register	0000 0010b
	PWM_DATA1	9Ch	PWM1 data register	xxxx xxxxb
	PWM_DATA2	9Bh	PWM2 data register	xxxx xxxxb
SPI0 related registers	SPI0_SETUP	FCh	SPI0 setting register	0000 0000b
	SPI0_S_PRE	FBh	SPI0 slave mode preset data register	0010 0000b
	SPI0_CK_SE	FBh	SPI0 clock frequency division setting register	0010 0000b
	SPI0_CTRL	FAh	SPI0 control register	0000 0010b
	SPI0_DATA	F9h	SPI0 data transmit and receive register	xxxx xxxxb
	SPI0_STAT	F8h	SPI0 state register	0000 1000b
UART1 related registers	SBAUD1	C2h	UART1 baud rate setting register	xxxx xxxxb
	SBUF1	C1h	UART1 data register	xxxx xxxxb
	SCON1	C0h	UART1 control register	0100 0000b
ADC related registers	ADC_DATA	9Fh	ADC data register	xxxx xxxxb
	ADC_CFG	9Ah	ADC configuration register	0000 0000b
	ADC_CTRL	80h	ADC control register	x000 0000b
Touch-Key related registers	TKEY_DATH	C5h	Touch-Key data high byte (read only)	0000 0000b
	TKEY_DATL	C4h	Touch-Key data low byte (read only)	xxxx xxxxb
	TKEY_DAT	C4h	TKEY_DATL and KEY_DATH constitute a 16-bit SFR	00xxh
	TKEY_CTRL	C3h	Touch-Key control register	x000 0000b
USB related registers	UEP1_DMA_H	EFh	Endpoint 1 buffer area start address high byte	0000 00xxb
	UEP1_DMA_L	EEh	Endpoint 1 buffer area start address low byte	xxxx xxxxb
	UEP1_DMA	EEh	UEP1_DMA_L and UEP1_DMA_H constitute a 16-bit SFR	0xxxh
	UEP0_DMA_H	EDh	Endpoint 0 and 4 buffer area start address high byte	0000 00xxb
	UEP0_DMA_L	ECh	Endpoint 0 and 4 buffer area start address low byte	xxxx xxxxb
	UEP0_DMA	ECh	UEP0_DMA_L and UEP0_DMA_H constitute a 16-bit SFR	0xxxh
	UEP2_3_MOD	EBh	Endpoint 2, 3 mode control register	0000 0000b
	UEP4_1_MOD	EAh	Endpoint 1, 4 mode control register	0000 0000b

	UEP3_DMA_H	E7h	Endpoint 3 buffer area start address high byte	0000 00xxb
	UEP3_DMA_L	E6h	Endpoint 3 buffer area start address low byte	xxxx xxxxb
	UEP3_DMA	E6h	UEP3_DMA_L and UEP3_DMA_H constitute a 16-bit SFR	0xxxh
	UEP2_DMA_H	E5h	Endpoint 2 buffer area start address high byte	0000 00xxb
	UEP2_DMA_L	E4h	Endpoint 2 buffer area start address low byte	xxxx xxxxb
	UEP2_DMA	E4h	UEP2_DMA_L and UEP2_DMA_H constitute a 16-bit SFR	0xxxh
	USB_DEV_AD	E3h	USB device address register	0000 0000b
	USB_CTRL	E2h	USB control register	0000 0110b
	USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
	UEP4_T_LEN	DFh	Endpoint 4 transmit length register	0xxx xxxxb
	UEP4_CTRL	DEh	Endpoint 4 control register	0000 0000b
	UEP0_T_LEN	DDh	Endpoint 0 transmit length register	0xxx xxxxb
	UEP0_CTRL	DCh	Endpoint 0 control register	0000 0000b
	USB_RX_LEN	DBh	USB receive length register (read only)	0xxx xxxxb
	USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
	USB_INT_ST	D9h	USB interrupt status register (read only)	00xx xxxxb
	USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
	UEP3_T_LEN	D7h	Endpoint 3 transmit length register	0xxx xxxxb
	UEP3_CTRL	D6h	Endpoint 3 control register	0000 0000b
	UEP2_T_LEN	D5h	Endpoint 2 transmit length register	0000 0000b
	UEP2_CTRL	D4h	Endpoint 2 control register	0000 0000b
	UEP1_T_LEN	D3h	Endpoint 1 transmit length register	0xxx xxxxb
	UEP1_CTRL	D2h	Endpoint 1 control register	0000 0000b
	UDEV_CTRL	D1h	USB device port control register	10xx 0000b
	USB_C_CTRL	91h	USB type-C configuration channel control register	0000 0000b

5.3 Universal 8051 Register

Table 5.3.1 Universal 8051 Register List

Name	Address	Description	Reset value
B	F0h	B register	00h
A, ACC	E0h	Accumulator	00h
PSW	D0h	Program state register	00h
GLOBAL_CFG	B1h	Global configuration register (in CH552 Bootloader state)	A0h
		Global configuration register (in CH552 application program state)	80h
		Global configuration register (in CH551 Bootloader state)	E0h
		Global configuration register (in CH551 application program	C0h

		state)	
CHIP_ID	A1h	ID code of CH552 (read only)	52h
		ID code of CH551 (read only)	51h
SAFE_MOD	A1h	Safe mode control register (write only)	00h
PCON	87h	Power supply control register (in power on reset state)	10h
DPH	83h	The higher 8 bits of data address pointer	00h
DPL	82h	The lower 8 bits of data address pointer	00h
DPTR	82h	DPL and DPH constitute a 16-bit SFR	0000h
SP	81h	Stack pointer	07h

B register (B):

Bit	Name	Access	Description	Reset value
[7:0]	B	RW	Arithmetic operation register, mainly used for multiplication and division operations, addressable by bit	00h

A accumulator (A, ACC):

Bit	Name	Access	Description	Reset value
[7:0]	A/ACC	RW	Arithmetic operation accumulator, addressable by bit	00h

Program state register (PSW):

Bit	Name	Access	Description	Reset value
7	CY	RW	Carry flag bit: used to record the carry or borrow of the highest bit when performing arithmetic operations and logical operations. In 8-bit addition operation, for the carry of the highest bit, the bit will be set, otherwise it will be cleared to 0. In 8-bit subtraction operation, for the borrow of the highest bit, the bit will be set, otherwise it will be cleared. The logical command can set or clear the bit	0
6	AC	RW	Auxiliary carry flag bit: Record that in addition and subtraction operations, for carry or borrow from the higher 4 bits to the lower 4 bits, AC will be set, otherwise it will be cleared.	0
5	F0	RW	Common flag bit 0 addressable by bit: user-defined, and can be cleared or set by software	0
4	RS1	RW	High bit of register bank selection bit	0
3	RS0	RW	Low bit of register bank selection bit	0
2	OV	RW	Overflow flag bit: in addition and subtraction operations, if the operation result exceeds 8-bit binary number, OV will be set as 1 and the flag will overflow, otherwise it will be cleared to 0.	0

1	F1	RW	Common flag bit 1 addressable by bit: user-defined, and can be cleared or set by software.	0
0	P	RO	Parity flag bit: record the parity of 1 in accumulator A after the command is executed, if the number of 1 is an odd number, P will be set. If the number of 1 is an even number, P will be cleared.	0

The state of processor is stored in the program state register PSW, and PSW supports be addressed by bit. The status word includes the carry flag bit, auxiliary carry flag bit for BCD code processing, parity flag bit, overflow flag bit, as well as RS0 and RS1 for working register bank selection.The area where the working register bank is located can be accessed directly or indirectly.

Table 5.3.2 RS1 and RS0 Working Register Bank Selection Table

RS1	RS0	Working register bank
0	0	Bank 0 (00h-07h)
0	1	Bank 1 (08h-0Fh)
1	0	Bank 2 (10h-17h)
1	1	Bank 3 (18h-1Fh)

Table 5.3.3 Operations Affecting Flag Bits (X Indicates that Flag Bit is related to the operation result)

Operation	CY	OV	AC	Operation	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

Data address pointer (DPTR):

Bit	Name	Access	Description	Reset value
[7:0]	DPL	RW	Data pointer low byte	00h
[7:0]	DPH	RW	Data pointer high byte	00h

DPL and DPH constitute a16-bit data pointer DPTR, which is used to access xRAM data memory or program memory. The actual DPTR corresponds to two sets of physical 16-bit data pointers of DPTR0 and DPTR1, which are dynamically selected by DPS in XBUS_AUX.

Stack pointer (SP):

Bit	Name	Access	Description	Reset value
[7:0]	SP	RW	Stack pointer, mainly used for program calls and interrupt calls as well as data in and out of the stack	07h

Specific function of stack: protect breakpoint and protect site, and carry out management on the principle of FIFO. During instack, SP pointer will automatically add 1, save the data or breakpoint information. During outstack, SP pointer will point to the data unit and automatically substract 1. The initial value of SP is 07h after reset, and the corresponding default stack storage starts from 08h.

5.4 Special Register

Global configuration register (GLOBAL_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	For CH552, it is the fixed value of 10	10b
[7:6]	Reserved	RO	For CH551, it is the fixed value of 11	11b
5	bBOOT_LOAD	RO	Bootloader state bit, used to distinguish ISP boot loader state or application state: set 1 during power on, and cleared to 0 during software reset. For the chip with ISP Bootloader, if the bit is 1, it indicates that it has never been reset by software and it is usually in the running state of ISP Bootloader after power on. If the bit is 0, it indicates that it has been reset by software, and it is usually in the application program state	1
4	bSW_RESET	RW	Software reset control bit: setting 1 will cause the software reset and automatic hardware reset	0
3	bCODE_WE	RW	Flash-ROM and DataFlash write permission bit: 0: Write protection. 1: Flash-ROM and Data can be rewritten.	0
2	bDATA_WE	RW	DataFlash area of Flash-ROM write permission bit: 0: Write protection. 1: DataFlash area can be rewritten.	0
1	bLDO3V3_OFF	RW	Disable control bit of USB power regulator LDO: 0: LDO is allowed, 3.3V voltage can be generated from 5V power for USB and internal clock oscillator. 1: LDO is disabled, and V33 pin must be supplied with external 3.3V power	0
0	bWDOG_EN	RW	Watchdog reset enable bit: 0: Watchdog is only used as timer. 1: Watchdog reset is allowed to be generated during timing overflow.	0

ID code of chip (CHIP_ID):

Bit	Name	Access	Description	Reset value
[7:0]	CHIP_ID	RO	For CH552, it is the fixed value of 52h to identify the chip	52h
[7:0]	CHIP_ID	RO	For CH551, it is the fixed value of 51h to identify the chip	51h

Safe mode control register (SAFE_MOD):

Bit	Name	Access	Description	Reset value
[7:0]	SAFE_MOD	WO	Used to enter or terminate safe mode	00h

Some SFRs can only be written in safe mode, while they are always read-only in non-safe mode. Steps to enter safe mode:

(1). Write 55h into this register;

(2). And then write AAh into this register;

(3). After that, about 13 to 23 dominant frequency cycles of the system are all in the safe mode, and one or more safe class SFR or ordinary SFR can be rewritten in such validity period;

(4). Automatic termination of the safe mode after the expiration of the above validity period;

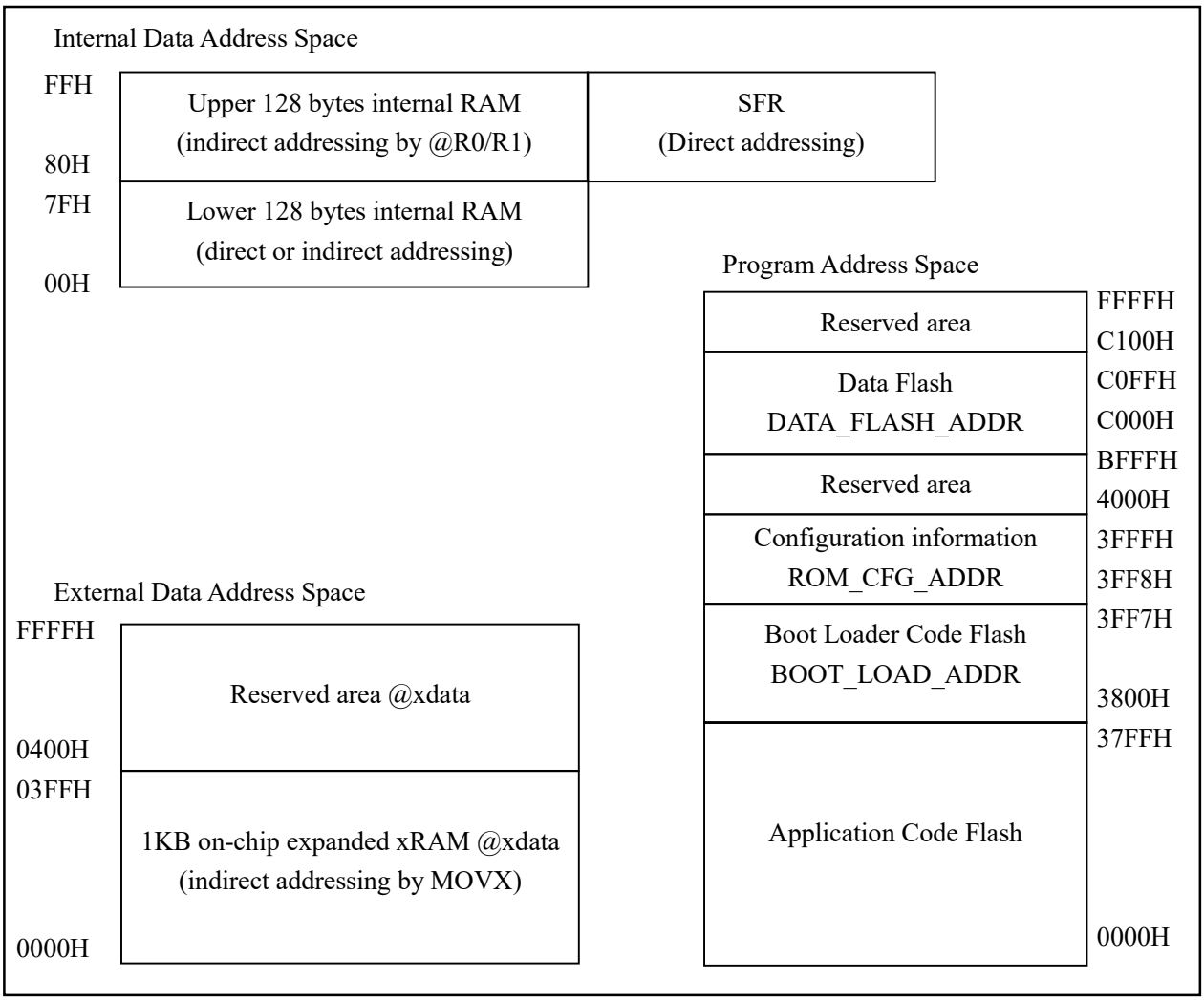
(5). Alternatively, writing any value to the register can prematurely terminate the safe mode.

6. Register Structure

6.1 Register Space

CH552 addressing space is divided into program storage space, internal data storage space and external data storage space.

Figure 6.1 Register Structure Chart



6.2 Program Storage Space

The program storage space is 64KB in total, as shown in Fugure 6.1, in which 16KB is used for ROM, including the Code Flash area to save the command code and the Configuration Information area.

Code Flash includes the application code for the low address area and the boot loader code for the high address area, or these two areas may be combined to save a single application code.

For CH551, the application code area of Code Flash is only 10KB.

ROM is an iFlash™ process, which can be programmed about 200 times under 5V power supply for the finished products after the formal packaging of blank ROM.

Data Flash address ranges from C000h to C0FFH (only the even address is valid, actually there is a memory cell every other byte), only supports single byte (8-bit) read and write operations, the data remains unchanged when the chip is powered off. Data Flash supports about 10,000 times writes, and balanced use is recommended. It is prohibited to write more than 10K to the same memory cell. For more writes, it is recommended to use CH558 or CH546/7.

Configuration Information includes 4 sets of 16-bit data located at the address from 3FF8H to 3FFFH, and the last three sets are read-only units that provide chip ID. The configuration data located at 3FF8H address is set by the programmer as required, refer to Table 6.2.

Table 6.2 flash-ROM Configuration Information Description

Bit address	Bit name	Description	Recommanded value
15	Code_Protect	Code and data protection mode in flash-ROM: 0- Forbid the programmer to read out, and keep the program secret; 1- Read enable	0/1
14	No_Boot_Load	Enable BootLoader start mode: 0- Start from the application from 0000h address; 1- Start from the boot loader from 3800h address	1
13	En_Long_Reset	Extra delay reset during enable power on reset: 0-standard short reset; 1-wide reset, extra 44mS reset time is added	0
12	En_RST_RESET	Enable RST pin as manual reset input pin: 0- Disable; 1 - Enable RST	0
[11:10]	Reserved	(Automatically set to 00 by the programmer as required)	00
9	Must_1	(Automatically set to 1 by the programmer as required)	1
8	Must_0	(Automatically set to 0 by the programmer as required)	0
[7:0]	All_1	(Automatically set to FFh by the programmer as required)	FFh

6.3 Data Storage Space

The internal data storage space, with 256 bytes in total, as shown in Fugure 6.1, has been all used for SFR and iRAM, in which iRAM is used for stack and fast temporary data storage, and can be subdivided into the working registers R0-R7, bit variable bdata, byte variable data and idata, etc.

External data storage space is 64KB in total, as shown in Figure 6.1. Part of it is used to expand xRAM within 1KB chip, and the remaining is reserved.

For CH551, the on-chip xRAM expansion is only 512 bytes.

6.4 flash-ROM Register

Table 6.4 flash-ROM Operation Register List

Name	Add:	Description	Reset value
ROM_DATA_H	8Fh	Flash-ROM data register high byte	xxh
ROM_DATA_L	8Eh	Flash-ROM data register low byte	xxh
ROM_DATA	8Eh	ROM_DATA_L and ROM_DATA_H constitute a 16-bit SFR	xxxxh
ROM_STATUS	86h	flash-ROM state register (read only)	00h
ROM_CTRL	86h	flash-ROM control register (write only)	00h
ROM_ADDR_H	85h	flash-ROM address register high byte	xxh
ROM_ADDR_L	84h	flash-ROM address register low byte	xxh
ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitute a 16-bit SFR	xxxxh

flash-ROM address register (ROM_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_ADDR_H	RW	Flash-ROM address high byte	xxh
[7:0]	ROM_ADDR_L	RW	Flash -ROM address low byte, only supports even addresses, For Data Flash, the actual offset adress of 00H-7fH must be shifted 1 bit left to become an even address of 00H/02H/04H...~ FEH and then re-insert.	xxh

flash-ROM data register (ROM_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DATA_H	RW	flash-ROM high bytes of data to be written	xxh
[7:0]	ROM_DATA_L	RW	flash-ROM low bytes of data to be written For DataFlash, they are data bytes to be written or read	xxh

flash-ROM control register (ROM_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_CTRL	WO	flash-ROM control register	00h

flash-ROM state register (ROM_STATUS):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0

6	bROM_ADDR_OK	RO	flash-ROM write operation address valid status bit: If the bit is 0, it indicates that the parameter is invalid. If the bit is 1, it indicates that the address is valid	0
[5:2]	Reserved	RO	Reserved	0000b
1	bROM_CMD_ERR	RO	flash-ROM operation command error status bit: If the bit is 0, it indicates that the command is valid. If the bit is 1, it indicates an unknown command	0
0	Reserved	RO	Reserved	0

6.5 flash-ROM Operation Steps

1. Write the flash-ROM code area to write the double bytes data to the target address:

(1). If the flash-ROM code is required to be written, 5V supply voltage must be selected;

(2). Enable safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(3). Set global configuration register GLOBAL_CFG to start write enable (bCODE_WE or bDATA_WE corresponding code or data);

(4). Set address register ROM_ADDR, write 16-bit target address (the lowest digit is always 0);

(5). Set data register ROM_DATA, write 16-bit data to be written, the sequence of step (4) and (5) can be alternative;

(6). Set operation control register ROM_CTRL as 09Ah, execute the write operation, and the program is automatically suspended during operation;

(7). After the operation is completed, the program will resume running. At this time, if you inquire the status register ROM_STATUS, you can check the status of the operation. If more than one data needs to be written, repeat the steps of (4), (5), (6) and (7);

(8). Re-enter the safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(9). Set global configuration register GLOBAL_CFG to start write protection (bCODE_WE=0, bDATA_WE=0);

2. Write the Data Flash data area to write the single byte data to the target address:

(1). Enable safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(2). Set global configuration register GLOBAL_CFG to start write enable (bDATA_WE corresponds data);

(3). Set address register ROM_ADDR, write 16-bit target address, and the actual offset adress of 00H-7FH must be shifted 1 bit left to become an even address of 00H/02H/04H...~FEH and then re-insert, and the final address is C000H/C002H/C004 in sequence...

(4). Set data register ROM_DATA_L, write 8-bit data to be written, the sequence of step (3) and (4) can be alternative;

(5). Set operation control register ROM_CTRL as 09Ah, execute the write operation, and the program is automatically suspended during operation;

(6). After the operation is completed, the program will resume running. At this time, if you inquire the status register ROM_STATUS, you can check the status of the operation. If more than one data needs to be written, repeat the steps of (3),(4), (5) and (6);

(7). Re-enter the safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(8). Set global configuration register GLOBAL_CFG to start write protection (bCODE_WE=0, bDATA_WE=0);

3. Read the Data Flash data area to read the single byte data from the target address:

(1). Set address register ROM_ADDR, write 16-bit target address, and the actual offset adress of 00H-7FH must be shifted 1 bit left to become an even address, and the final address is C000H/C002H/C004 in sequence...
(2). Set operation control register ROM_CTRL as 08Eh, execute the read operation, and the program is automatically suspended during operation;
(3). After the operation is completed, the program will resume running. At this time, if you inquire bROM_CMD_ERR in the status register ROM_STATUS, you can check the status of the operation. If the command is valid, the read 8-bit data will be saved in the data register ROM_DATA_L;
(4). If more than one data needs to be read, repeat the steps of (1), (2) and (3).

4. Read flash-ROM:
Directly use MOVC command, or read the code or data of the target address through the pointer to the program storage space.

6.6 On-board Programming and ISP Downloading

When the configuration information Code_Protect=1, the code in CH552 chip flash-ROM and the data in Data Flash can be read and written by an external programmer through the synchronous serial interface. When the configuration information Code_Protect=0, the code in the flash-ROM and the data in Data Flash are protected and cannot be read out, but can be erased, and the code protection will be removed when the code is erased and powered on again.

When the CH552 chip is preset with BootLoader program, it supports various ISP downloading ways such as USB or asynchronous serial port to load the applications. But in the absence of a boot loader program, CH552 can only be written to the boot loader program or application by an external dedicated programmer. To support on-board programming, 5V supply voltage must be used temporarily, and 4 connecting pins between the CH552 and the programmer should be reserved in the circuit. The minimum number of necessary connecting pins are 3: P1.4, P1.6 and P1.7.

Table 6.6.1 Connecting Pin to Programmer

Pin	GPIO	Pin description
RST	RST	Reset control pin in programming state, it is allowed to enter the programming state at high level
SCS	P1.4	Chip selection input pin in programming state (necessary), high level by default, active at low level
SCK	P1.7	Clock input pin in programming state (necessary)
MISO	P1.6	Data input pin in programming state (necessary)

Notes: Whether programming on board or downloading programs via serial port or USB, 5V supply voltage must be used temporarily.

6.7 Unique ID Number of Chip

Each MCU has a unique ID when it is delivered from the factory, namely the chip identification number. The ID data is 5 bytes in total and stored in the address from 3FFAH to 3FFFH of Configuration Information area. The address 3FFBH is reserved. The address 3FFCH and address 3FFEH each occupies 16 bits and the address 3FFAH occupies 8 bits, and they are combined into 40-bit chip ID..

Table 6.7.1 Chip ID Address Table

Program space address	ID data description
3FFAh, 3FFBh	ID last word data, correspond to the highest byte of the 40-bit ID number and the reserved byte
3FFCh, 3FFDh	ID first word data, correspond to the lowest byte of the ID number and the second lowest byte
3FFEh, 3FFFh	ID secondary word data, correspond to the secondary high byte of the ID number and the high byte

This ID can be obtained by reading the Code Flash. The ID number can be used with the downloading tools to encrypt the target program. For the general application, only the first 32 bits of the ID number are used, i.e. the 8-bit data of the 3FFAH address can be ignored.

7. Power Management, Sleep and Reset

7.1 External Power Input

CH552 chip has built-in low dropout voltage regulator of 5V to 3.3V, it supports external 5V or 3.3V or even 2.8V supply voltage input. Refer to the following table for the two supply voltage input modes.

External supply voltage	VCC pin voltage: external voltage 3V~5V	V33 pin voltage: internal voltage 3.3V
3.3V or 3V Including less than 3.6V	Input external 3.3V voltage to voltage regulator, The decoupling capacitance no less than 0.1uF must be connected to the ground	Input external 3.3V as internal working power supply, The decoupling capacitance no less than 0.1uF must be connected to the ground
5V Including more than 3.6V	Input external 5V voltage to voltage regulator, The decoupling capacitance no less than 0.1uF must be connected to the ground	Internal voltage regulator 3.3V output And 3.3V internal working power supply input, The decoupling capacitance no less than 0.1uF must be connected to the ground

After power on or system reset, CH552 is in running state by default. On the premise that the performance meets the requirements, the power consumption can be reduced during operation by appropriately reducing the dominant frequency of the system. When CH552 does not need to run at all, PD in PCON can be set to enter the sleep state. In the sleep state, external waking can be conducted via USB, UART0, UART1, SPI0 and part of GPIOs.

7.2 Power Supply and Sleep Control Register

Table 7.2.1 Power Supply and Sleep Control Register List

Name	Address	Description	Reset value
WDOG_COUNT	FFh	Watchdog count register	00h
RESET_KEEP	FEh	Reset keep register	00h
WAKE_CTRL	A9h	Sleep wake-up control register	00h
PCON	87h	Power control register	10h

Watchdog count register (WDOG_COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	WDOG_COUNT	RW	Current count of watchdog, it will overflow when the count is full from 0FFh to 00h, and it will automatically set the interrupt flag bWDOG_IF_TO to 1 during overflow	00h

Reset keep register (RESET_KEEP):

Bit	Name	Access	Description	Reset value
[7:0]	RESET_KEEP	RW	For the reset keep register, the value can be modified manually and will not be affected by any other reset except for the reset by power on reset	00h

Sleep wake-up control register (WAKE_CTRL), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bWAK_BY_USB	RW	USB event wake-up enable; the waking is forbidden if the bit is 0	0
6	bWAK_RXD1_LO	RW	UART1 receive input low level waking enable; the waking is forbidden if the bit is 0. Select either RXD1 or RXD1_ based on bUART1_PIN_X=0/1	0
5	bWAK_P1_5_LO	RW	P1.5 low level waking enable; the waking is forbidden if the bit is 0	0
4	bWAK_P1_4_LO	RW	P1.4 low level waking enable; the waking is forbidden if the bit is 0	0
3	bWAK_P1_3_LO	RW	P1.3 low level waking enable; the waking is forbidden if the bit is 0	0
2	bWAK_RST_HI	RW	RST high level waking enable; the waking is forbidden if the bit is 0	0
1	bWAK_P3_2E_3L	RW	P3.2 edge change and P3.3 low level waking enable; the waking is forbidden if the bit is 0	0
0	bWAK_RXD0_LO	RW	UART0 receive input low level waking enable; the waking is forbidden if the bit is 0. Select either RXD0 or RXD0_ pin based on bUART0_PIN_X=0/1	0

Power control register (PCON):

Bit	Name	Access	Description	Reset value
7	SMOD	RW	When the UART0 baud rate is generated by timer 1, select the communication baud rate of UART10 mode 1, 2 and 3: 0-slow mode; 1-fast mode	0
6	Reserved	RO	Reserved	0

5	bRST_FLAG1	RO	Last reset flag high bit of chip	0
4	bRST_FLAG0	RO	Last reset flag low bit of chip	1
3	GF1	RW	Common flag bit 1: user-defined, and can be cleared or set by software	0
2	GF0	RW	Common flag bit 0: user-defined, and can be cleared or set by software	0
1	PD	RW	Sleep mode enabled, sleep after set 1, automatically cleared to 0 by hardware after waking	0
0	Reserved	RO	Reserved	0

Table 7.2.2 Last Reset Flag Description of Chip

bRST_FLAG1	bRST_FLAG0	Reset flag description
0	0	Software reset, source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1)
0	1	Power on reset, source: VCC pin voltage lower than detection level
1	0	Watchdog reset, source: bWDOG_EN=1 and watchdog timeout overflows
1	1	External pin manual reset, source: En_RST_RESET=1 and RST input high level

7.3 Reset Control

CH552 has 4 reset sources: power on reset, external reset, software reset, watchdog reset, and the last three are thermal reset.

7.3.1 Power on Reset

The power on reset (POR) is generated by the on-chip voltage detection circuit. The POR circuit continuously monitors the supply voltage of VCC pin. When it is lower than the detection level Vpot, the power on reset will be generated, and the hardware will automatically delay Tpor to remain the reset state. After the delay, the CH552 will run.

Only power on reset can enable CH552 to reload the configuration information and reset RESET_KEEP, other thermal reset is not affected.

7.3.2 External Reset

The external reset is generated by the high level applied to the RST pin. The reset process is triggered when the configuration information En_RST_RESET is 1, and the high level duration on the RST pin is greater than Trst. When the external high level signal is canceled, the hardware will automatically delay Trdl to remain the reset state. After the delay, CH552 will be executed from address 0.

7.3.3 Software Reset

CH552 supports internal software reset, so that the CPU state can be actively reset and re-run without external intervention. Set bSW_RESET in global configuration register GLOBAL_CFG to 1 to reset the software, and automatically delay Trdl to remain the reset state. After the delay, CH552 will be executed from address 0, and the bSW_RESET bit will be reset automatically by the hardware.

When bSW_RESET is set to 1, if bBOOT_LOAD=0 or bWDOG_EN=1, then bRST_FLAG1/0 after reset

will indicate a software reset. When bSW_RESET is set to 1, if bBOOT_LOAD=1 and bWDOG_EN=0, then bRST_FLAG1/0 will remain the previous reset flag rather than generate a new one.

For a chip with ISP boot loader, after power on reset of power, firstly run the boot loader, and the program will reset the chip via software as needed to switch to the application state. Such software reset only cause reset of bBOOT_LOAD, and do not affect bRST_FLAG1/0 state (due to bBOOT_LOAD = 1 before reset), so when switching to the application state, bRST_FLAG1/0 still indicate the power on reset state.

7.3.4 Watchdog Reset

Watchdog reset is generated when the watchdog timer overflows. The watchdog timer is an 8-bit counter, whose clock frequency of its counts is the dominant frequency of the system Fsys/65536, and the overflow signal will be generated when the count reaches 0FFh to 00h.

The watchdog timer overflow signal will trigger an interrupt flag bWDOG_IF_TO as 1, which is automatically reset when WDOG_COUNT is reloaded or entering the corresponding interrupt service program.

Different timing cycles Twdc are realized by writing different counting initial values to WDOG_COUNT. At the dominant frequency of 6MHz, the watchdog timing cycle Twdc is about 2.8 s when 00h is written, and about 1.4 s when 80h is written. The timing cycle is halved at the dominant frequency of 12MHz.

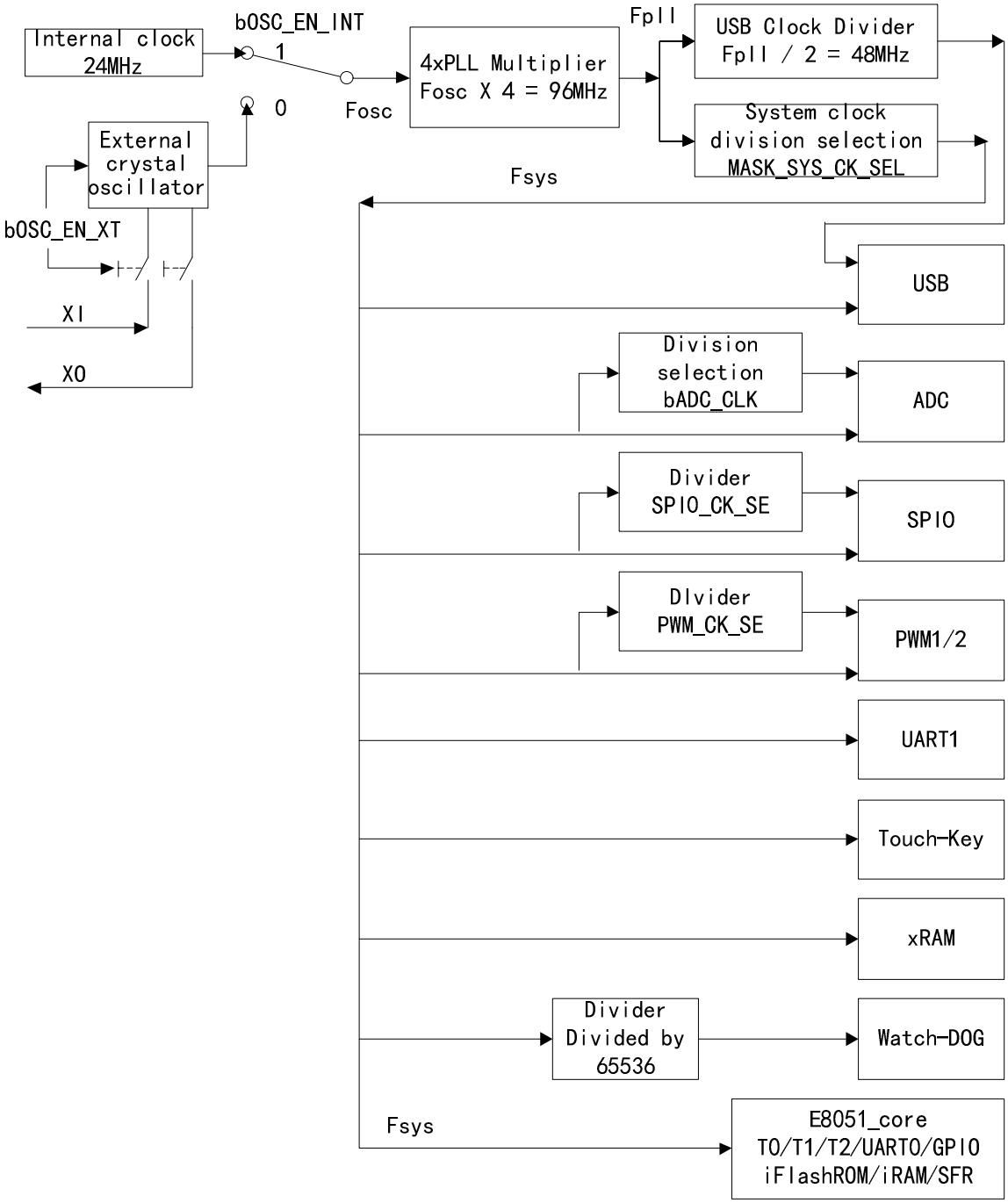
If bWDOG_EN=1 when watchdog timer overflows, watchdog reset will be generated and Trdl will be automatically delayed to remain the reset state. After the delay, CH552 will be executed from address 0.

When bWDOG_EN=1, to avoid being reset by the watchdog, WDOG_COUNT must be reset timely to avoid its overflow.

8. System Clock

8.1 Clock Block Diagram

Figure 8.1.1 Clock System and Structure Chart



After the internal clock or external clock is alternatively selected as the original clock Fosc, Fpll high frequency clock is generated after 4xPLL frequency multiplier, and finally the system clock Fsys and USB module clock Fusb4x are respectively obtained via the two groups of frequency dividers. System clock Fsys is directly provided to each module of CH552.

8.2 Register Description

Table 8.2.1 Clock Control Register List

Name	Address	Description	Reset value
CLOCK_CFG	B9h	System clock configuration register	83h

System clock configuration register (CLOCK_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bOSC_EN_INT	RW	Internal clock oscillator enable, if the bit is 1, enable the internal clock oscillator and select the internal clock. If the bit is 0, turn off the internal clock oscillator and select the external crystal oscillator to provide the clock	1
6	bOSC_EN_XT	RW	External crystal oscillator enable. The P1.2/P1.3 pin is used as XI/XO and the oscillator is enabled if the bit is 1, and quartz crystal or ceramic oscillator needs to be externally connected between the XI and XO. Turn off the external oscillator if the bit is 0	0
5	bWDOG_IF_TO	RO	Watch dog timer interrupt flag. If the bit is 1, it indicates that there is an interrupt triggered by the timer overflow signal. If the bit is 0, it indicates that there is no interrupt. The bit will be automatically reset when the watchdog count register WDOG_COUNT is reloaded or after entering the corresponding interrupt service program	0
4	bROM_CLK_FAST	RW	flash-ROM reference clock frequency selection: 0- normal (if Fosc>=16MHz); 1- Speed up (if Fosc<16MHz)	0
3	bRST	RO	RST pin state input bit	0
[2:0]	MASK_SYS_CK_SEL	RW	System clock frequency selection, refer to the Table 8.2.2 below	011b

Table 8.2.2 System Dominant Frequency Selection Table

MASK_SYS_CK_SEL	System dominant frequency Fsys	Relation with crystal frequency Fxt	Fsys when Fosc=24MHz
000	Fpll / 512	Fxt / 128	187.5KHz
001	Fpll / 128	Fxt / 32	750KHz
010	Fpll / 32	Fxt / 8	3MHz
011	Fpll / 16	Fxt / 4	6MHz
100	Fpll / 8	Fxt / 2	12MHz
101	Fpll / 6	Fxt / 1.5	16MHz
110	Fpll / 4	Fxt / 1	24MHz
111	Fpll / 3	Fxt / 0.75	Reserved, disabled

8.3 Clock Configuration

The internal clock is used by default after the CH552 chip is powered on, and the internal clock frequency is 24MHz. An internal clock or external crystal oscillator clock can be selected through CLOCK_CFG. If the external crystal oscillator is turned off, the XI and XO pins can be used as P1.2 and P1.3 common I/O ports. If an external crystal oscillator is used to provide the clock, the crystal should be cross connected

between the XI and XO pins, and the oscillating capacitance should be connected for the GND between the XI and XO pins respectively. If the clock signal is input directly from the outside, it should be input from the XI pin with the XO pin suspended.

Original clock frequency Fosc = bOSC_EN_INT ? 24MHz: Fxt
PLL frequency Fpll = Fosc * 4 = 96MHz
USB clock frequency Fusb4x = Fpll / 2 = 48MHz
The system dominant frequency Fsys Reference Table 8.2.2 is obtained by Fpll frequency division
In default state after reset, Fosc=24MHz, Fpll=96MHz, Fusb4x=48MHz, and Fsys=6MHz.

Steps for switching to the external crystal oscillator to provide the clock are as follows:
(1). Enter the safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;
(2). Set bOSC_EN_XT in CLOCK_CFG to 1 with a "or by bit" operation, other bits remain unchanged, and enable crystal oscillator;
(3). Delay several milliseconds, usually 5mS ~ 10mS, waiting for the crystal oscillator to work steadily;
(4). Re-enter the safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;
(5). Reset bOSC_EN_INT in CLOCK_CFG to 0 with a "and by bit" operation, other bits remain unchanged, and switch to external clock;
(6). Turn off the safe mode, write any value into SAFE_MOD to prematurely terminate the safe mode.

Steps for modifying the system dominant frequency are as follows:
(1). Enter the safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;
(2). Write new value to CLOCK_CFG;
(3). Turn off the safe mode, write any value into SAFE_MOD to prematurely terminate the safe mode.

Remarks:
(1). If the USB module is used, the Fusb4x must be 48MHz; in addition, when the full speed USB is used, the system dominant frequency Fsys is not less than 6MHz; when the low speed USB is used, the system dominant frequency Fsys is not less than 1.5mhz.
(2). A lower system clock frequency Fsys is preferred to be used to reduce the system dynamic power consumption and widen the operating temperature range.
(3). The internal clock oscillator is powered by a V33 power, so V33 voltage variations, especially low voltages will affect the internal clock frequency.

9. Interrupt

CH552 chip supports 14 sets of interrupt signal sources, including 6 sets of interrupts compatible with the standard MCS51: INT0, T0, INT1, T1, UART0, T2, and 8 sets of extended interrupts: SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG, in which GPIO interrupt can be selected from 7 I/O pins.

9.1 Register Description

Table 9.1.1 Interrupt Vector Table

Interrupt sources	Entry address	Interrupt number	Description	Default priority sequence
INT_NO_INT0	0x0003	0	External interrupt 0	High priority
INT_NO_TMR0	0x000B	1	Timer 0 interrupt	↓

INT_NO_INT1	0x0013	2	External interrupt 1	↓
INT_NO_TMR1	0x001B	3	Timer 1 interrupt	↓
INT_NO_UART0	0x0023	4	UART0 interrupt	↓
INT_NO_TMR2	0x002B	5	Timer 2 interrupt	↓
INT_NO_SPI0	0x0033	6	SPI0 interrupt	↓
INT_NO_TKEY	0x003B	7	Touch key timer interrupt	↓
INT_NO_USB	0x0043	8	USB interrupt	↓
INT_NO_ADC	0x004B	9	ADC interrupt	↓
INT_NO_UART1	0x0053	10	UART1 interrupt	↓
INT_NO_PWMX	0x005B	11	PWM1/PWM2 interrupt	↓
INT_NO_GPIO	0x0063	12	GPIO Interrupt	↓ Low priority
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	

Table 9.1.2 List of Interrupt Related Registers

Name	Address	Description	Reset value
IP_EX	E9h	Extend interrupt priority control register	00h
IE_EX	E8h	Extend interrupt enable register	00h
GPIO_IE	C7h	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority control register	00h
IE	A8h	Interrupt enable register	00h

Interrupt enable register (IE):

Bit	Name	Access	Description	Reset value
7	EA	RW	Global interrupt enable control bit, if the bit is 1 and E_DIS is 0, it allows interrupt. If the bit is 0, it shields all interrupts requests	0
6	E_DIS	RW	Global interrupt disable control bit, if the bit is 1, it shields all interrupts requests. If the bit is 0 and EA is 1, it allows interrupt. This bit is usually used for temporary disable interrupt during flash-ROM operation	0
5	ET2	RW	Timer 2 interrupt enable bit, if the bit is 1, it allows T2 interrupt. If the bit is 0, it indicates shielding	0
4	ES	RW	UART0 interrupt enable bit, if the bit is 1, it allows UART0 interrupt. If the bit is 0, it indicates shielding	0
3	ET1	RW	Timer 1 interrupt enable bit, if the bit is 1, it allows T1 interrupt. If the bit is 0, it indicates shielding	0
2	EX1	RW	External interrupt 1 enable bit, if the bit is 1, it allows INT1 interrupt. If the bit is 0, it indicates shielding	0
1	ET0	RW	Timer 0 interrupt enable bit, if the bit is 1, it allows T0 interrupt. If the bit is 0, it indicates shielding	0
0	EX0	RW	External interrupt 0 enable bit, if the bit is 1, it allows INT0 interrupt. If the bit is 0, it indicates shielding	0

Extend interrupt enable register (IE_EX):

Bit	Name	Access	Description	Reset value
7	IE_WDOG	RW	Watchdog timer interrupt enable bit, if the bit is 1, it allows WDOG interrupt. If the bit is 0, it indicates shielding	0
6	IE_GPIO	RW	GPIO interrupt enable bit, if the bit is 1, it allows enable interrupt in GPIO_IE. If the bit is 0, it shields all interrupts in GPIO_IE	0
5	IE_PWMX	RW	PWM1/PWM2 interrupt enable bit, if the bit is 1, it allows PWM1/2 interrupt. If the bit is 0, it indicates shielding	0
4	IE_UART1	RW	UART1 interrupt enable bit, if the bit is 1, it allows UART1 interrupt. If the bit is 0, it indicates shielding	0
3	IE_ADC	RW	ADC anolog digital conversion interrupt enable bit, if the bit is 1, it allows ADC interrupt. If the bit is 0, it indicates shielding	0
2	IE_USB	RW	USB interrupt enable bit, if the bit is 1, it allows USB interrupt. If the bit is 0, it indicates shielding	0
1	IE_TKEY	RW	Touch key timer interrupt enable bit, if the bit is 1, it allows timing interrupt. If the bit is 0, it indicates shielding	0
0	IE_SPI0	RW	SPI0 interrupt enable bit, if the bit is 1, it allows SPI0 interrupt. If the bit is 0, it indicates shielding	0

GPIO interrupt enable register (GPIO_IE):

Bit	Name	Access	Description	Reset value
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: If the bit is 0, select level interrupt mode. If the GPIO pin inputs the valid level, bIO_INT_ACT will be 1 and always request interrupt. If the GPIO inputs invalid level, bIO_INT_ACT will be 0 and cancel the interrupt request. If the bit is 1, select the edge interrupt mode. When GPIO pin inputs valid edge, an interrupt flag bIO_INT_ACT will be generated and an interrupt is requested. The interrupt flag cannot be reset by software and can only be reset automatically in reset or level interrupt mode or when entering the corresponding interrupt service program	0
6	bIE_RXD1_LO	RW	If the bit is 1, it enables UART1 receive pin interrupt (active at low level in level mode, while active at falling edge in edge mode). If the bit is 0, it indicates forbidden. Select either RXD1 or RXD1_ based on bUART1_PIN_X=0/1	0

5	bIE_P1_5_LO	RW	If the bit is 1, it enables P1.5 interrupt (active at low level in level mode, while active at falling edge in edge mode). If the bit is 0, it indicates forbidden	0
4	bIE_P1_4_LO	RW	If the bit is 1, it enables P1.4 interrupt (active at low level in level mode, while active at falling edge in edge mode). If the bit is 0, it indicates forbidden	0
3	bIE_P1_3_LO	RW	If the bit is 1, it enables P1.3 interrupt (active at low level in level mode, while active at falling edge in edge mode). If the bit is 0, it indicates forbidden	0
2	bIE_RST_HI	RW	If the bit is 1, it enables RST interrupt (active at high level in level mode, while active at rising edge in edge mode). If the bit is 0, it indicates forbidden	0
1	bIE_P3_1_LO	RW	If the bit is 1, it enables P3.1 interrupt (active at low level in level mode, while active at falling edge in edge mode). If the bit is 0, it indicates forbidden	0
0	bIE_RXD0_LO	RW	If the bit is 1, it enables UART0 receive pin interrupt (active at low level in level mode, while active at falling edge in edge mode). If the bit is 0, it indicates forbidden. Select either RXD0 or RXD0_ pin based on bUART0_PIN_X=0/1	0

Interrupt priority control register (IP):

Bit	Name	Access	Description	Reset value
7	PH_FLAG	RO	Flag bit for high-priority interrupt in progress	0
6	PL_FLAG	RO	Flag bit for low-priority interrupt in progress	0
5	PT2	RW	Timer 2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer 1 interrupt priority control bit	0
2	PX1	RW	External interrupt 1 interrupt priority control bit	0
1	PT0	RW	Timer 0 interrupt priority control bit	0
0	PX0	RW	External interrupt 0 interrupt priority control bit	0

Extend interrupt priority control register (IP_EX):

Bit	Name	Access	Description	Reset value
7	bIP_LEVEL	RO	Current interrupt nesting level flag bit, if the bit is 0, it indicates no interrupt or nesting level 2 interrupt. If the bit is 1, it indicates current nesting level 1 interrupt	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWMX	RW	PWM1/PWM2 interrupt priority control bit	0
4	bIP_UART1	RW	UART1 interrupt priority control bit	0
3	bIP_ADC	RW	ADC interrupt priority control bit	0
2	bIP_USB	RW	USB interrupt priority control bit	0

1	bIP_TKEY	RW	Touch key timer interrupt priority control bit	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

IP and IP_EX registers are used to set the interrupt priority, if some bit is set to 1, then the corresponding interrupt source is set to be the high priority. If some bit is reset to 0, then the corresponding interrupt source is set to be the low priority. For the interrupt source at the same level, the system has a priority sequence by default, as shown in Table 9.1.1. Among which the combination of PH_FLAG and PL_FLAG represents the priority of the current interrupt.

Table 9.1.3 Current Interrupt Priority State Indication

PH_FLAG	PL_FLAG	Interrupt priority state at present
0	0	No interrupt at present
0	1	Low priority interrupt is executing at present
1	0	High priority interrupt is executing at present
1	1	Unexpected state, unknown error

10. I/O Port

10.1 Introduction of GPIO

CH552 provides up to 17 I/O pins, some of which have multiplex function. Among which, the input and output of ports P1 and P3 can be addressable by bit. Port P2 is the internal port and is only used to cooperate with R0 or R1 to select the xRAM page for MOVX access.

If the pin is not configured with the multiplexing function, it is the common I/O pin state by default. When used as a common digital I/O, all I/O ports have a real "read-modify-write" function that allows SETB or CLR equipotential operation commands to independently change the direction of certain pins or port level.

10.2 GPIO Register

All registers and bits in this section are represented in a general format: a lowercase "n" represents the serial number of the port (n=1 or 3), and a lowercase "x" represents the serial number of the bit (x=0, 1, 2, 3, 4, 5, 6, 7).

Table 10.2.1 List of GPIO Register

Name	Address	Description	Reset value
P1	90h	P1 port input and output register	FFh
P1_MOD_OC	92h	P1 port output mode register	FFh
P1_DIR_PU	93h	P1 port direction control and pull-up enable register	FFh
P2	A0h	P2 port output register	FFh
P3	B0h	P3 port input and output register	FFh
P3_MOD_OC	96h	P3 port output mode register	FFh
P3_DIR_PU	97h	P3 port direction control and pull-up enable register	FFh
PIN_FUNC	C6h	Pin function selection register	80h
XBUS_AUX	A2h	Bus auxiliary setting register	00h

Pn port input and output register (Pn):

Bit	Name	Access	Description	Reset value
[7:0]	Pn.0~Pn.7	RW	Pn.x pin state input and data output bits, addressable by bit	FFh

Pn port output mode register (Pn_MOD_OC):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_MOD_OC	RW	Pn.x pin output mode setting: 0- push-pull output; 1- open-drain output	FFh

Pn port direction control and pull-up enable register (Pn_DIR_PU):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_DIR_PU	RW	Pn.x pin direction control in push-pull output mode: 0- input; 1- output; Pn.x pin pull-up resistor enable control in open-drain output mode: 0- disable the pull-up resistor; 1- enable the pull-up resistor;	FFh

Relevant configuration of Pn port is realized by the combination of Pn_MOD_OC[x] and Pn_DIR_PU[x] as follows.

Table 10.2.2 Port Configuration Register Combination

Pn_MOD_OC	Pn_DIR_PU	Working mode description
0	0	High impedance input mode, pin has no pull-up resistor
0	1	Push-pull output mode, has symmetrical drive capability which can output or absorb large current
1	0	Open-drain output, support high impedance input, pin has no pull-up resistor
1	1	Quasi-bidirectional mode (standard 8051), open-drain output, support input, pin has pull-up resistor, when the output is changed from low level to high level, it will automatically drive the high level of 2 clock cycles to accelerate the conversion

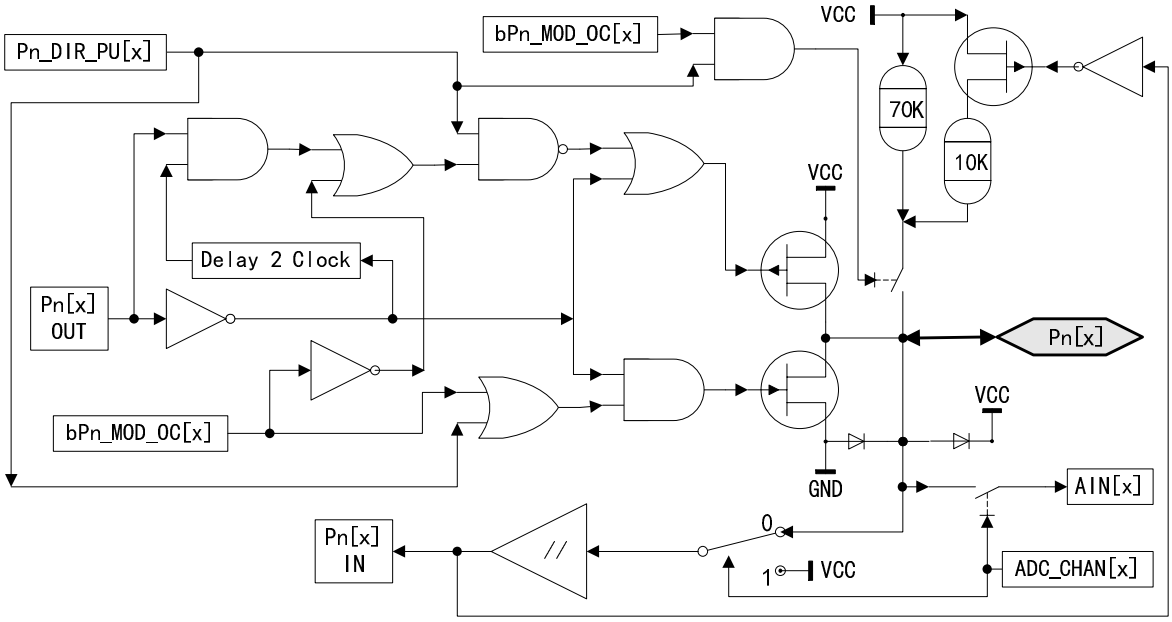
Ports P1 and P3 support pure input or push-pull output and quasi-bidirectional modes, etc. Each pin has a freely controlled internal pull-up resistor, and a protective diode connected to VCC and GND.

Figure 10.2.1 is the equivalent schematic diagram of pin P1.x of port P1. After AIN is removed, it can be applied to port P3. The VCC in the figure can be applied to P3.6 and P3.7 after changed to V33, that is, the pull-up or input or output high level of P3.6 and P3.7 can only reach V33 voltage.

P3.6 and P3.7 optional standard pull-up resistor (to V33), 15KΩ pull-down resistor, or provide 1.5KΩ pull-up resistor for one pin (to V33). The standard pull-up resistor is only valid when bUSB_IO_EN=0, i.e. in GPIO mode, controlled by bit 7 and bit 6 of P3_DIR_PU. The pull-down resistor is controlled by

bUD_PD_DIS when bUC_RESET_SIE=0, and has no connection with bUSB_IO_EN. 1.5KΩ pull-up resistor is prior to the pull-down resistor, controlled by bUC_DEV_PU_EN when bUC_RESET_SIE = 0, and has no connection with bUSB_IO_EN.

Figure 10.2.1 I/O Pin Equivalent Schematic Diagram



10.3 GPIO Multiplex and Mapping

Some I/O pins of CH552 have the function of multiplexing. After power on, they are all general purpose I/O pins by default. After enabling different functional modules, the corresponding pins are configured as corresponding functional pins of each functional module.

Pin function selection register (PIN_FUNC):

Bit	Name	Access	Description	Reset value
7	bUSB_IO_EN	RW	USB UDP/UDM pin enable bit, P3.6/P3.7 is used for GPIO if the bit is 0, support P3_DIR_PU control pull-up resistor, and support P3_MOD_OC. If the bit is 1, P3.6/P3.7 is used for UDP/UDM, controlled by USB module, and P3_DIR_PU and P3_MOD_OC are invalid to it	1
6	bIO_INT_ACT	RO	GPIO interrupt request activation status: When bIE_IO_EDGE=0, if the bit is 1, it indicates that GPIO inputs valid level and interrupts the request. If the bit is 0, it indicates that the input level is invalid; When bIE_IO_EDGE=1, the bit is used as the edge interrupt flag, if the bit is 1, it indicates that the effective edge is detected and the bit cannot be reset by software and can only be reset automatically in reset or level interrupt mode or when entering the corresponding interrupt service program	0

5	bUART1_PIN_X	RW	UART1 pin mapping enable bit, if the bit is 0, RXD1/TXD1 uses P1.6/P1.7. If the bit is 1, RXD1/TXD1 uses P3.4/P3.2	0
4	bUART0_PIN_X	RW	UART0 pin mapping enable bit, if the bit is 0, RXD0/TXD0 uses P3.0/P3.1. If the bit is 1, RXD0/TXD0 uses P1.2/P1.3	0
3	bPWM2_PIN_X	RW	PWM2 pin mapping enable bit, if the bit is 0, PWM2 uses P3.4. If the bit is 1, PWM2 uses P3.1	0
2	bPWM1_PIN_X	RW	PWM1 pin mapping enable bit, if the bit is 0, PWM1 uses P1.5. If the bit is 1, PWM1 uses P3.0	0
1	bT2EX_PIN_X	RW	T2EX/CAP2 pin mapping enable bit, if the bit is 0, T2EX/CAP2 uses P1.1. If the bit is 1, T2EX/CAP2 uses RST	0
0	bT2_PIN_X	RW	T2/CAP1 pin mapping enable bit, if the bit is 0, T2/CAP1 uses P1.0. If the bit is 1, T2/CAP1 uses P1.4	0

Table 10.4.1 GPIO Pin Multiplex Function List

GPIO	Other functions: priority sequence from left to right
RST	RST, bT2EX_, bCAP2_, bRST
P1[0]	T2/bT2, CAP1/bCAP1, TIN0, P1.0
P1[1]	T2EX/bT2EX, CAP2/bCAP2, TIN1, VBUS2, AIN0, P1.1
P1[2]	XI, RXD_/bRXD_, P1.2
P1[3]	XO, TXD_/bTXD_, P1.3
P1[4]	T2_/bT2_, CAP1_/bCAP1_, SCS/bSCS, TIN2, UCC1, AIN1, P1.4
P1[5]	MOSI/bMOSI, PWM1/bPWM1, TIN3, UCC2, AIN2, P1.5
P1[6]	MISO/bMISO, RXD1/bRXD1, TIN4, P1.6
P1[7]	SCK/bSCK, TXD1/bTXD1, TIN5, P1.7
P3[0]	PWM1_/bPWM1_, RXD/bRXD, P3.0
P3[1]	PWM2_/bPWM2_, TXD/bTXD, P3.1
P3[2]	TXD1_/bTXD1_, INT0/bINT0, VBUS1, AIN3, P3.2
P3[3]	INT1/bINT1, P3.3
P3[4]	PWM2/bPWM2, RXD1_/bRXD1_, T0/bT0, P3.4
P3[5]	T1/bT1, P3.5
P3[6]	UDP/bUDP, P3.6
P3[7]	UDM/bUDM, P3.7

The priority sequence from left to right mentioned in the above table refers to the priority when multiple functional modules compete to use the GPIO. For example, when P3.1 is used for TXD serial port transmission, P3.0 can still be used for higher priority PWM1 output.

11. External Bus

CH552 does not provide bus signals outside the chip, does not support the external bus, but can normally access the on-chip xRAM.

External bus auxiliary setting register (XBUS_AUX):

Bit	Name	Access	Description	Reset value
7	bUART0_TX	RO	It indicates the transmission status of UART0, if the bit is 1, it indicates that the transmission is in progress	0
6	bUART0_RX	RO	It indicates the reception status of UART0, if the bit is 1, it indicates that the reception is in progress	0
5	bSAFE_MOD_ACT	RO	It indicates the safe mode status, if the bit is 1, it indicates that it is in safe mode currently	0
4	Reserved	RO	Reserved	0
3	GF2	RW	Common flag bit 2. The users can define it by their own, and reset or set by software	0
2	bDPTR_AUTO_INC	RW	Enable the DPTR to add 1 automatically after on the completion of MOVX_@DPTR command	0
1	Reserved	RO	Reserved	0
0	DPS	RW	Double DPTR data pointer selection bit: If the bit is 0, select DPTR0. If the bit is 1, select DPTR1	0

12. Timer

12.1 Timer0/1

Timer0 and Timer1 are 16-bit timers/counters configured by TCON and TMOD. TCON is used for timer/counter T0 and T1 startup control and overflow interrupt as well as external interrupt control. Each timer is a 16-bit timing unit composed of 2 8-bit registers. The high byte counter of timer 0 is TH0 and the low byte is TL0. The high byte counter for timer 1 is TH1 and the low byte is TL1. Timer 1 can also be used as the baud rate generator of UART0.

Table 12.1.1 List of Timer0/1 Related Registers

Name	Address	Description	Reset value
TH1	8Dh	Timer 1 count high byte	xxh
TH0	8Ch	Timer 0 count high byte	xxh
TL1	8Bh	Timer 1 count low byte	xxh
TL0	8Ah	Timer 0 count low byte	xxh
TMOD	89h	Timer0/1 mode register	00h
TCON	88h	Timer0/1 control register	00h

Timer/counter 0/1 control register (TCON):

Bit	Name	Access	Description	Reset value
7	TF1	RW	Timer1 overflow interrupt flag bit, automatic reset after entering Timer1 interrupt	0
6	TR1	RW	Timer1 startup/stop bit, set 1 to start, set or reset by software	0
5	TF0	RW	Timer0 overflow interrupt flag bit, automatic reset after entering Timer0 interrupt	0
4	TR0	RW	Timer0 startup/stop bit, set 1 to start, set or reset by software	0

3	IE1	RW	Interrupt request flag bit of INT1 external interrupt 1, automatic reset after entering interrupt	0
2	IT1	RW	Trigger mode control bit of INT1 external interrupt 1, if the bit is 0, select low level trigger for external interrupt. If the bit is 1, select falling edge trigger for external interrupt	0
1	IE0	RW	Interrupt request flag bit of INT0 external interrupt 0, automatic reset after entering interrupt	0
0	IT0	RW	Trigger mode control bit of INT0 external interrupt 0, if the bit is 0, select low level trigger for external interrupt. If the bit is 1, select falling trigger for external interrupt	0

Timer/counter 0/1 mode register (TMOD):

Bit	Name	Access	Description	Reset value
7	bT1_GATE	RW	Door control enable bit controls whether the Timer1boot is affected by the external interrupt signal INT1. If the bit is 0, whether the timer/counter 1 is started is independent of INT1. If the bit is 1, it can only be started when the INT1 pin is in high level and TR1 is 1	0
6	bT1_CT	RW	Timing or counting mode selection bit, if the bit is 0, it works in timing mode. If the bit is 1, it works in counting mode, and uses the falling edge of T1 pin as the clock	0
5	bT1_M1	RW	Timer/counter 1 mode selection high bit	0
4	bT1_M0	RW	Timer/counter 1 mode selection low bit	0
3	bT0_GATE	RW	Door control enable bit controls whether the Timer0 boot is affected by the external interrupt signal INT0. If the bit is 0, whether the timer/counter 0 is started is independent of INT0. If the bit is 1, it can only be started when the INT0 pin is in high level and TR1 is 0	0
2	bT0_CT	RW	Timing or counting mode selection bit, if the bit is 0, it works in timing mode. If the bit is 1, it works in counting mode, and uses the falling edge of T0 pin as the clock	0
1	bT0_M1	RW	Timer/counter 0 mode selection high bit	0
0	bT0_M0	RW	Timer/counter 0 mode selection low bit	0

Table 12.1.2 bTn_M1 and bTn_M0 Select Timern Working Mode (n=0,1)

bTn_M1	bTn_M0	Timern working mode (n=0,1)
0	0	Mode 0: 13-bit timer/counter n, the counting unit is composed of the lower 5 bits of TLn and THn, and the higher 3 bits of TLn is invalid. When the count changes from 1 to 0 of all 13 bits, set the overflow flag TFn and reset the initial value
0	1	Mode 1: 16-bit timer/counter n, the counting unit is composed of TLn and THn. When the count changes from 1 to 0 of all 16 bits, set the overflow flag TFn and reset the initial value
1	0	Mode 2: 8-bit overload timer/counter n, TLn is used for the counting unit, and THn is

		used as the overload counting unit. When the count changes from 1 to 0 of all 8 bits, set the overflow flag TFn and automatically load the initial value from THn
1	1	Mode 3: If it is timer/counter 0, then timer/counter 0 is divided into 2 parts, TL0 and TH0. TL0 is used as 8-bit timer/counter, occupying all control bits of Timer0. TH0 is also used as another 8-bit timer, occupying TR1, TF1 and interrupt resources of Timer1. At this time, Timer1 is still available, but the startup control bit TR1 and overflow flag bit TF1 cannot be used. If it is timer/counter 1, it will enter mode 3 and stop timer/counter 1.

Timern count low byte (TLn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	TLn	RW	Timern count low byte	xxh

Timern count high byte (THn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	THn	RW	Timern count high byte	xxh

12.2 Timer2

Timer2 is a 16-bit automatic overload timer/counter configured via T2CON and T2MOD registers, with the high byte counter being TH2 and the low byte being TL2 for Timer2.Timer2 can be used as the baud rate generator of UART0, and it also has the function of 2-channel signal level capture. The capture count is stored in RCAP2 and T2CAP1 registers.

Table 12.2.1 List of Timer2 Related Register

Name	Address	Description	Reset value
TH2	CDh	Timer 2 counter high byte	00h
TL2	CCh	Timer 2 counter low byte	00h
T2COUNT	CCh	TL2 and TH2 constitute a 16-bit SFR	0000h
T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	xxh
T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxh
T2CAP1	CEh	T2CAP1L and T2CAP1H constitute a 16-bit SFR	xxxxh
RCAP2H	CBh	Count reload/capature 2 data register high byte	00h
RCAP2L	CAh	Count reload/capature 2 data register low byte	00h
RCAP2	CAh	RCAP2L and RCAP2H constitute a 16-bit SFR	0000h
T2MOD	C9h	Timer2 mode register	00h
T2CON	C8h	Timer2 control register	00h

Timer/counter 2 control register (T2CON):

Bit	Name	Access	Description	Reset value
7	TF2	RW	When bT2_CAP1_EN=0, it is the Timer2 overflow interrupt flag, when the Timer2 count changes from all 1 to	0

			all 0 of 16 bits, the overflow flag is set as 1, which requires the software to reset. When RCLK=1 or TCLK=1, the bit will not be set to 1	
7	CAP1F	RW	When bT2_CAP1_EN=1, it is the Timer2 capture 1 interrupt flag, which is triggered by the effective edge of T2, which requires software to reset it	0
6	EXF2	RW	Timer2 external trigger flag, when EXEN2=1, T2EX effective edge trigger set as 1, which requires software to reset	0
5	RCLK	RW	UART0 receive clock selection, if the bit is 0, select Timer1 overflow pulse to generate the baud rate. If the bit is 1, select Timer2 overflow pulse to generate the baud rate	0
4	TCLK	RW	UART0 transmit clock selection, if the bit is 0, select Timer1 overflow pulse to generate the baud rate. If the bit is 1, select Timer2 overflow pulse to generate the baud rate	0
3	EXEN2	RW	T2EX trigger enable bit, if the bit is 0, ignore T2EX. If the bit is 1, enable overload or capture to be triggered in T2EX effective edge	0
2	TR2	RW	Timer2 startup/stop bit, set 1 to start, set or reset by software	0
1	C_T2	RW	Timer2 clock source selection bit, if the bit is 0, use the internal clock. If the bit is 1, use the edge counting based on T2 pin falling edge	0
0	CP_RL2	RW	Timer2 function selection bit, which should be forced to be 0 if RCLK or TCLK is 1. If the bit is 0, Timer2 is used as timer/counter to automatically reload the initial value of the count when the counter overflows or T2EX level changes. If the bit is 1, enable Timer2 capture 2 function, and capture the effective edge of T2EX	0

Timer/counter 2 mode register (T2MOD):

Bit	Name	Access	Description	Reset value
7	bTMR_CLK	RW	The fastest clock mode enable of T0/T1/T2 timer of the selected fast clock, if the bit is 1, use the dominant frequency Fsys of the system without frequency division as the counting clock. If the bit is 0, use the clock with frequency division. This bit has no affect on the timer that selects the standard clock	0
6	bT2_CLK	RW	Timer2 internal clock frequency selection bit, if the bit is 0, select the standard clock, timer/counter mode is Fsys/12, and UART0 clock mode is Fsys/4. If the bit is 1, select the fast clock, timer/counter mode is Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1), and UART0 clock mode is Fsys/2 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)	0

5	bT1_CLK	RW	Timer1 internal clock frequency selection bit, if the bit is 0, select the standard clock Fsys/12. If the bit is 1, select the fast clock Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)		0
4	bT0_CLK	RW	Timer0 internal clock frequency selection bit, if the bit is 0, select the standard clock Fsys/12. If the bit is 1, select the fast clock Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)		0
3	bT2_CAP_M1	RW	Timer2 capture mode high bit	Capture mode selection: X0: from falling ege to falling edge 01: from any edge to any edge, i.e. level change 11: from rising edge to rising edge	0
2	bT2_CAP_M0	RW	Timer2 capture mode low bit		0
1	T2OE	RW	Timer2 clock output enable bit, if the bit is 0, disable output. If the bit is 1, enable T2 pin output clock, and the frequency is the half of the Timer2 overflow rate		0
0	bT2_CAP1_EN	RW	Capture 1 mode enable when RCLK=0, TCLK=0, CP_RL2=1, C_T2=0, T2OE=0, if the bit is 1, enable capture 1 function to capture the effective edge of T2. If the bit is 0, disable capture 1		0

Count reload/capature 2 data register (RCAP2):

Bit	Name	Access	Description	Reset value
[7:0]	RCAP2H	RW	High byte of reload value in timer/counter mode. High byte of timer captured by CAP2 in capture mode	00h
[7:0]	RCAP2L	RW	Low byte of reload value in timer/counter mode. Low byte of timer captured by CAP2 in capture mode	00h

Timer2 counter (T2COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	TH2	RW	Current counter high byte	00h
[7:0]	TL2	RW	Current counter low byte	00h

Timer2 capture 1 data (T2CAP0):

Bit	Name	Access	Description	Reset value
[7:0]	T2CAP1H	RO	High byte of timer captured by CAP1	xxh
[7:0]	T2CAP1L	RO	Low byte of timer captured by CAP1	xxh

12.3 PWM Function

CH552 provides 2-channel 8-bit PWM, the default output polarity can be selected by default as low level or high level for PWM, and the output duty cycle of PWM can be dynamically modified. After integrating

low-pass filtering via simple Resistor-Capacitor (RC), various output voltages can be obtained, which is equivalent to the low speed Digital Analog Converter (DAC).

PWM1 output duty cycle= PWM_DATA1 / 256, support range from 0% to 99.6%.
PWM2 output duty cycle= PWM_DATA2 / 256, support range from 0% to 99.6%.

In practical application, it is recommended to allow the PWM pin output and set the PWM output pin in push-pull output mode.

12.3.1 PWM1 and PWM2

Table 12.3.1 Relevant Registers List of PWM1 and PWM2

Name	Address	Description	Reset value
PWM_CK_SE	9Eh	PWM clock frequency division setting register	00h
PWM_CTRL	9Dh	PWM control register	02h
PWM_DATA1	9Ch	PWM1 data register	xxh
PWM_DATA2	9Bh	PWM2 data register	xxh

PWM2 data register (PWM_DATA2):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_DATA2	RW	Store the current PWM2 data, Duty cycle of PWM2 output effective level =PWM_DATA2/256	xxh

PWM1 data register (PWM_DATA1):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_DATA1	RW	Store the current PWM1 data, Duty cycle of PWM1 output effective level =PWM_DATA1/256	xxh

PWM control register (PWM_CTRL):

Bit	Name	Access	Description	Reset value
7	bPWM_IE_END	RW	If the bit is 1, it enables PWM cycle end or MFM buffer interrupt	0
6	bPWM2_POLAR	RW	The output polarity of PWM2 is controlled. If the bit is 0, low level by default while active at high level. If the bit is 1, high level by default while active at low level.	0
5	bPWM1_POLAR	RW	The output polarity of PWM1 is controlled. If the bit is 0, low level by default while active at high level. If the bit is 1, high level by default while active at low level	0
4	bPWM_IF_END	RW	The interrupt flag bit at the end of the PWM cycle. If the bit is 1, it indicates that there is interrupt. If the bit is 1, it can be reset when reset or reload the PWM_DATA1 data	0

3	bPWM2_OUT_EN	RW	PWM2 output enable, if the bit is 1, enable PWM2 output	0
2	bPWM1_OUT_EN	RW	PWM1 output enable, if the bit is 1, enable PWM1 output	0
1	bPWM_CLR_ALL	RW	If the bit is 1, empty PWM1 and PWM2 counts and FIFO, and software is required to reset	1
0	Reserved	RO	Reserved	0

PWM clock frequency division setting register (PWM_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_CK_SE	RW	Set PWM clock frequency division divisor	00h

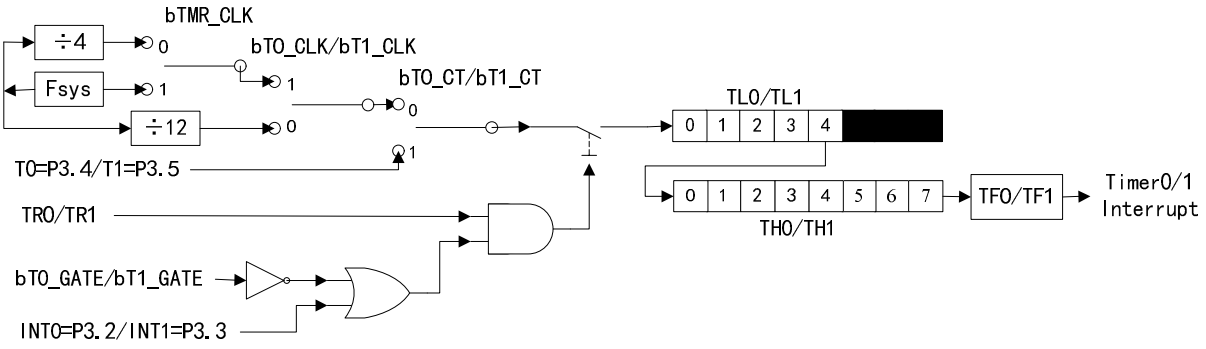
12.4 Timer Function

12.4.1 Timer0/1

(1). Set T2MOD, select Timer internal clock frequency, if bTn_CLK(n=0/1) is 0, then the corresponding clock of Timer0/1 is Fsys/12. If bTn_CLK is 1, then bTMR_CLK=0 or 1 selects Fsys/4 or Fsys as the clock.

(2). Set TMOD to configure the working mode of Timer.

Mode 0: 13-bit timer/counter



Fugure 12.4.1.1 Timer0/1 Mode 0

Mode 1: 16-bit timer/counter

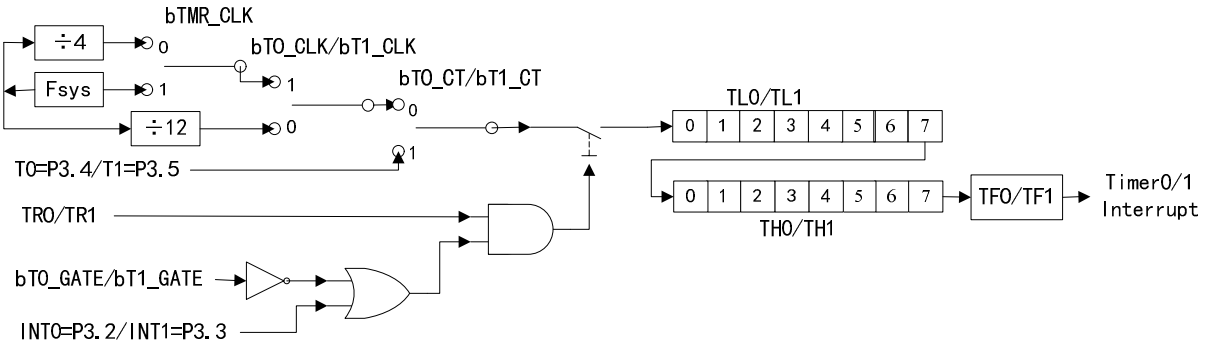
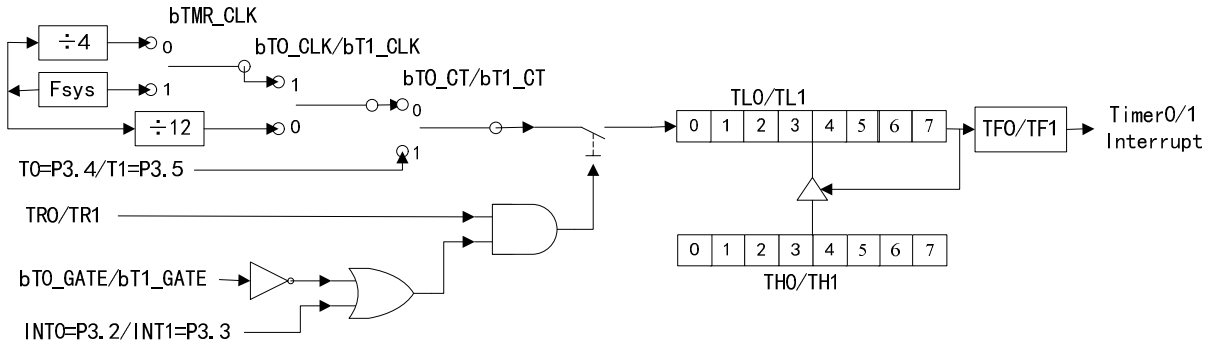


Figure 12.4.1.2 Timer0/1 Mode 1

Mode 2: automatic reload 8-bit timer/counter



Fugure 12.4.1.3 Timer0/1 Mode 2

Mode 3: Timer0 is divided into two independent 8-bit timer/counter and borrows the TR1 control bit of Timer1. Timer1 substitutes the borrowed TR1 control bit by whether starting mode 3, and stops running when it enters mode 3.

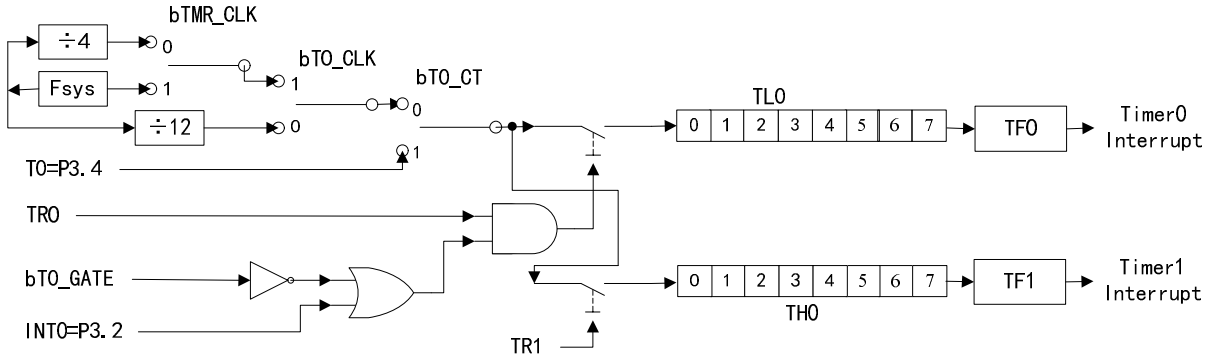


Figure 12.4.1.4 Timer0 Mode 3

(3). Set initial value TLn and THn(n=0/1) of timer/counter.

(4). Set the bit TRn(n=0/1) in TCON to turn on or stop timer/counter, which can be checked by bit TFn(n=0/1) query or by interrupt mode.

12.4.2 Timer2

Timer2 16-bit reload timer/counter mode:

(1). Set the bit RCLK and TCLK in T2CON to 0, and select the non-serial port baud rate generator mode.

(2). Set the bit C_T2 in T2CON to 0, select to use the internal clock, and turn to step (3). Alternatively, set 1 to select the falling edge of T2 pin as the count clock and skip step (3).

(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, then Timer2 clock is Fsys/12. If bT2_CLK is 1, then Fsys/4 or Fsys is selected as the clock by bTMR_CLK=0 or 1.

(4). Set bit CP_RL2 of T2CON to 0, and select 16-bit reload timer/counter function of Timer2.

(5). Set RCAP2L and RCAP2H as the reload value of timer after overflow, set TL2 and TH2 as the initial value of the timer (generally it is the same as RCAP2L and RCAP2H), set TR2 to 1 and turn on Timer2.

(6). Inquire TF2 or Timer2 interrupt to obtain the current timer/counter state.

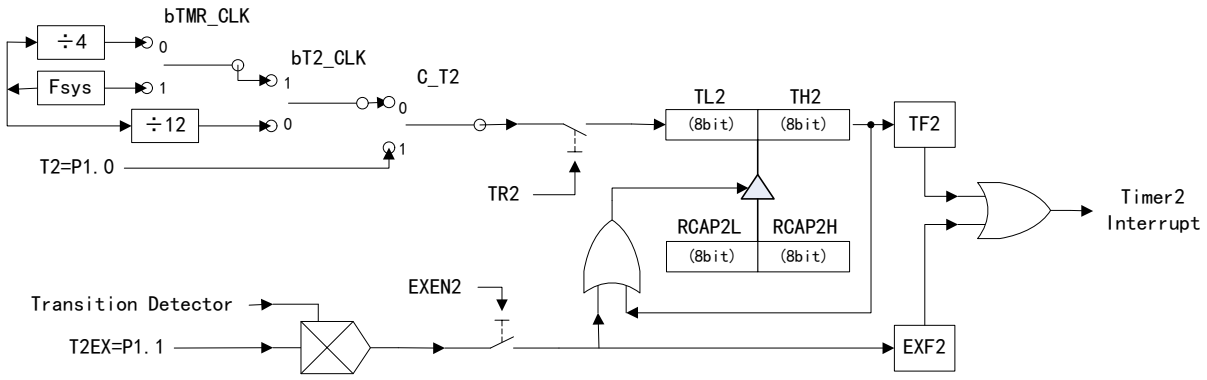


Figure 12.4.2.1 Timer2 16-bit Reload Timer/Counter

Timer2 clock output mode:

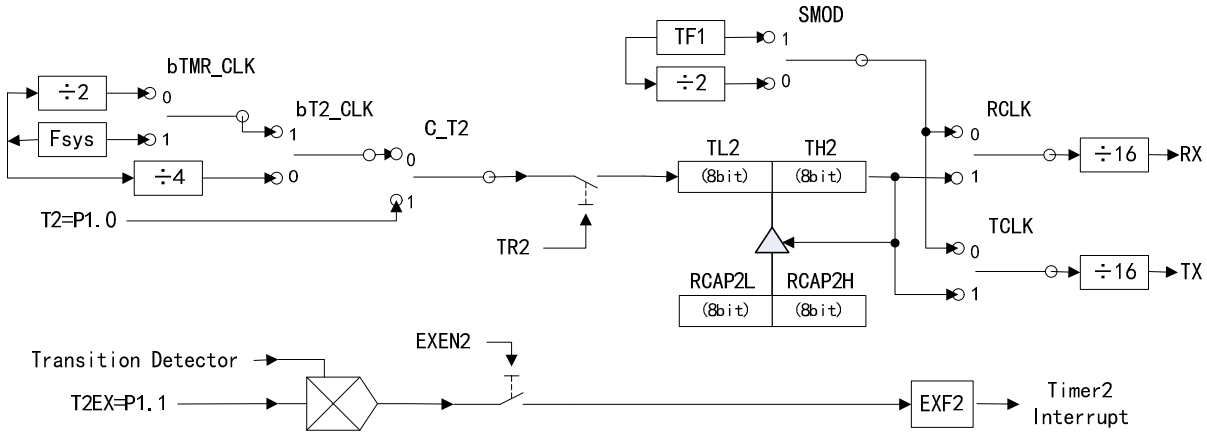
Refer to the 16-bit reload timer/counter mode and then set the bit T2OE in T2MOD to 1 to enable a two divided-frequency clock of TF2 frequency output from T2 pin.

Timer2 UART0 baud rate generator mode:

(1). Set the bit C_T2 in T2CON to 0, select to use the internal clock, alternatively, set 1 to select the falling edge of T2 pin as the clock, set the bit RCLK and TCLK in T2CON to 1 or one of them to 1 as required, and select the serial port baud rate generator mode.

(2). Set T2MOD, select Timer internal clock frequency, if bT2_CLK is 0, then the clock of Timer2 is Fsys/4. If bT2_CLK is 1, then bTMR_CLK=0 or 1 selects Fsys/2 or Fsys as the clock.

(3). Set RCAP2L and RCAP2H as the reload value of timer after overflow, set TR2 to 1 and turn on Timer2.



Fugure 12.4.2.2 Timer2 UART0 Baud Rate Generator

Timer2 two-channel capture mode:

(1). Set the bit RCLK and TCLK in T2CON to 0, and select the non-serial port baud rate generator mode.

(2). Set the bit C_T2 in T2CON to 0, select to use the internal clock, and turn to step (3). Alternatively, set 1 to select the falling edge of T2 pin as the count clock and skip step (3).

(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, then Timer2 clock is Fsys/12. If bT2_CLK is 1, then Fsys/4 or Fsys is selected as the clock by bTMR_CLK=0 or 1.

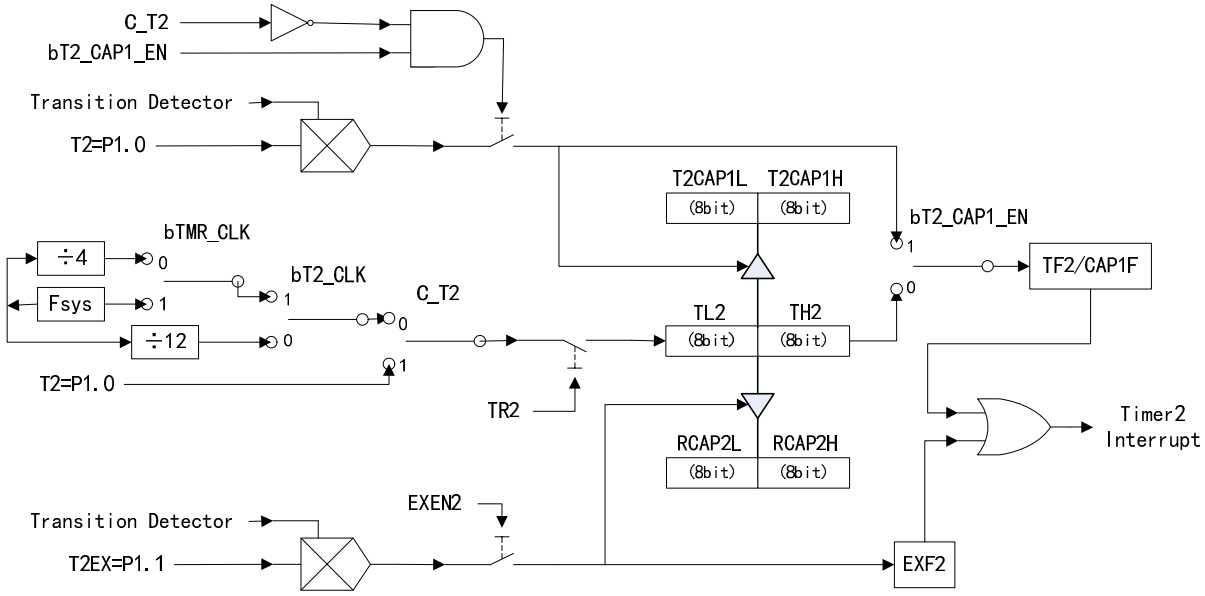
(4). Set the bit bT2_CAP_M1 and bT2_CAP_M0 in T2MOD, and select corresponding edge capture mode.

(5). Set the bit CP_RL2 in T2CON to 1, and select the capture function of Timer2 to T2EX pin.

(6). Set TL2 and TH2 as the initial value of the timer, and set TR2 to 1 and turn on Timer2.

(7). When CAP2 capture is completed, RCAP2L and RCAP2H will save the current count values of TL2 and TH2 and set EXF2 to generate an interrupt. The difference between the next captured RCAP2L and RCAP2H and the last captured RCAP2L and RCAP2H is the signal width between the two effective edges.

(8). If the bit C_T2 in T2CON is 0, and the bit bT2_CAP1_EN in T2MOD is 1, Timer2 will be enabled to capture the T2 pin at the same time. When the CAP1 capture is completed, T2CAP1L and T2CAP1H will save the current count values of TL2 and TH2, and set CAP1F to generate an interrupt.



Fugure 12.4.2.3 Timer2 Capture Mode

13. Universal Asynchronous Receiver/Transmitter, UART

13.1 Introduction of UART

CH552 chip provides 2 full-duplex UARTs: UART0 and UART1. CH551 only provides UART0.

UART0 is a standard MCS51 serial port, whose data reception and transmission are realized by physically separated receive/transmit registers via SBUF access. The data written to SBUF is loaded into the transmit register, and the read operation to SBUF corresponds to the receive buffer register.

UART1 is a simplified MCS51 serial port, whose data reception and transmission are realized by physically separated receive/transmit registers via SBUF access. The data written to SBUF1 is loaded into the transmit register, and the read operation to SBUF1 corresponds to the receive buffer register. Compared with UART0, UART1 has removed the multi-device communication mode and fixed baud rate with independent baud rate generator.

13.2 UART Register

Table 13.2.1 List of UART Related Register

Name	Address	Description	Reset value
SCON	98h	UART0 control register	00h
SBUF	99h	UART0 data register	xxh
SCON1	C0h	UART1 control register	40h
SBUF1	C1h	UART1 data register	xxh

SBAUD1	C2h	UART1 baud rate setting register	xxh

13.2.1 UART0 Register Description

UART0 control register (SCON):

Bit	Name	Access	Description	Reset value
7	SM0	RW	UART0 working mode selection bit, if the bit is 0, select 8-bit data asynchronous communication. If the bit is 1, select 9-bit data asynchronous communication	0
6	SM1	RW	UART0 working mode selection bit 1, if the bit is 0, set fixed baud rate. If the bit is 1, set variable baud rate, which is generated by timer T1 or T2	0
5	SM2	RW	UART0 multi-device communication control bit: When receiving data in mode 2 and 3 and SM2=1, if RB8 is 0, then RI will not be set to 1 and the reception is invalid. If RB8 is 1, then RI is set to 1 and the reception is valid. When SM2=0, no matter RB8 is 0 or 1, RI is set when receiving data and the reception is valid; In mode 1, if SM2=1, only when the effective stop bit is received can the receiving be valid; In mode 0, the bit SM2 must be set to 0	0
4	REN	RW	UART0 allow receive control bit, if the bit is 0, it indicates receiving forbidden. If the bit is 1, it allows receive	0
3	TB8	RW	The 9th bit of data transmitted, in modes 2 and 3, TB8 is used to write the 9th bit of data transmitted, which can be a parity bit. In multi-machine communication, it is used to indicate whether the host sends an address byte or a data byte, TB8=0 is the data, and TB8=1 is the address	0
2	RB8	RW	The 9th bit of data received, in mode 2 and 3, RB8 is used to store the 9th bit of data received. In mode 1, if SM2=0, then RB8 is used to store the received stop bit. In mode 0, RB8 is not used	0
1	TI	RW	Transmit interrupt flag bit, a data byte is set by hardware after transmission, which requires software to reset	0
0	RI	RW	Receive interrupt flag bit, a data byte is set by hardware after effective reception, which requires software to reset	0

Table 13.2.1.1 UART0 Working Mode Selection

SM0	SM1	Description
0	0	Mode 0, shift register mode, baud rate is fixed to be Fsys/12
0	1	Mode 1, 8-bit asynchronous communication way, variable baud rate, generated by timer T1 or T2
1	0	Mode 2, 9-bit asynchronous communication way, baud rate is Fsys/128(SMOD=0) or Fsys/32(SMOD=1)

1	1	Mode 3, 9-bit asynchronous communication way, variable baud rate, generated by timer T1 or T2

In mode 1 and 3, when RCLK=0 and TCLK=0, UART0 baud rate is generated by timer T1. T1 should be set as mode 2 automatic reload 8-bit timer mode, both bT1_CT and bT1_GATE must be 0. There are the following clock types.

Table 13.2.1.2 Calculation Formula of UART0 Baud Rate Generated from T1

bTMR_CLK	bT1_CLK	SMOD	Description
1	1	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In mode 1 and 3, when RCLK=1 or TCLK=1, UART0 baud rate is generated by timer T2. T2 should be set as 16-bit automatic reload baud rate generator mode, both C_T2 and CP_RL2 must be 0. There are the following clock types.

Table 13.2.1.3 Calculation Formula of UART0 Baud Rate Generated from T2

bTMR_CLK	bT2_CLK	Description
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 data register (SBUF):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF	RW	UART0 data register, including the transmit and receive registers that are physically separated. Write data to SBUF correspond to transmit data register. Read data from SBUF correspond to receive data register	xxh

13.2.2 UART1 Register Description

UART1 control register (SCON1):

Bit	Name	Access	Description	Reset value
7	U1SM0	RW	UART1 working mode selection bit, if the bit is 0, select 8-bit data asynchronous communication. If the bit is 1, select 9-bit data asynchronous communication	0
6	Reserved	RO	Reserved	1
5	U1SMOD	RW	Select communication baud rate of UART1: 0-slow mode; 1-fast mode	0
4	U1REN	RW	UART1 allow receive control bit, if the bit is 0, it indicates	0

			receiving forbidden. If the bit is 1, it allows receive.	
3	U1TB8	RW	The 9th bit of data transmitted, in 9-bit data mode, TB8 is used to write the 9th bit of data transmitted, which can be a parity bit. In 8-bit data mode, TB8 is ignored	0
2	U1RB8	RW	The 9th bit of data received, in 9-bit data mode, RB8 is used to store the 9th bit of data received. In 8-bit data mode, RB8 is used to store the received stop bit	0
1	U1TI	RW	Transmit interrupt flag bit, a data byte is set by hardware after being sent, which requires software to reset	0
0	U1RI	RW	Receive interrupt flag bit, a data byte is set by hardware after being received effectively, which requires software to reset	0

UART1 Baud rate is generated by the SBAUD1 setting and can be divided into two cases according to the selection of U1SMOD:

When U1SMOD=0, SBAUD1 = 256 - Fsys / 32 / baud rate;
When U1SMOD=1, SBAUD1 = 256 - Fsys / 16 / baud rate.

UART1 data register (SBUF1):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF1	RW	UART1 data register, including the transmit and receive registers that are physically separated. Write data to SBUF1 correspond to transmit data register. Read data from SBUF1 correspond to receive data register	xxh

13.3 UART Application

UART0 Application:

(1). Select UART0 baud rate generator, either from timer T1 or T2, and configure the corresponding counter.

(2). Turn on the timer T1 or T2.

(3).Set SM0, SM1, SM2 of SCON to select the working mode of UART0. Set REN as 1 and enable UART0 receiving.

(4). UART interrupt can be set or R1 and T1 interrupt state can be inquired.

(5). Read and write SBUF to realize data reception and transmission of UART, and the allowable baud rate error of UART receive signal is not more than 2%.

UART1 application:

(1). Select U1SMOD and set SBAUD1 based on the baud rate.

(2).Set U1SM0 of SCON1 to select the working mode of UART1. Set U1REN as 1 and enable UART1 receiving.

(3). UART1 interrupt can be set or U1RI and U1TI interrupt state can be inquired.

(4). Read and write SBUF1 to realize data reception and transmission of UART1, and the allowable baud rate error of UART receive signal is not more than 2%.

14. Synchronous Serial Interface, SPI

14.1 SPI Introduction

CH552 chip provides an SPI interface for high-speed synchronous data transmission with peripherals.

(1). Support master mode and slave mode;

(2). Support clock modes of mode 0 and mode 3;

(3). Optional 3-line full duplex or 2-line half-duplex mode;

(4). Optional MSB high bit is sent first or LSB low bit is sent first;

(5). Clock frequency is adjustable, up to nearly half of the dominant frequency of the system;

(6). Built-in 1-byte receiver FIFO and 1-byte transmitter FIFO;

(7). Support the first byte pre-load data in slave mode to facilitate the host to obtain the returned data immediately in the first byte.

14.2 SPI Register

Table 14.2.1 List of SPI Related Register

Name	Address	Description	Reset value
SPI0_SETUP	FCh	SPI0 register	00h
SPI0_S_PRE	FBh	SPI0 slave mode preset data register	20h
SPI0_CK_SE	FBh	SPI0 clock frequency division setting register	20h
SPI0_CTRL	FAh	SPI0 control register	02h
SPI0_DATA	F9h	SPI0 data receive/transmit register	xxh
SPI0_STAT	F8h	SPI0 state register	08h

SPI0 setting register (SPI0_SETUP):

Bit	Name	Access	Description	Reset value
7	bS0_MODE_SLV	RW	SPI0 master slave mode selection bit, if the bit is 0, SPI0 is in master mode. If the bit is 1, SPI0 is in slave mode/device mode	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable bit in slave mode, if the bit is 1, it enables FIFO overflow interrupt. If the bit is 0, FIFO overflows but not generates interrupt	0
5	bS0_IE_FIRST	RW	Receive first byte complete interrupt enable bit in slave mode, if the bit is 1, the interrupt is trigger when the first data byte is received in slave mode. If the bit is 0, the interrupt will not be generated when the first byte is received	0
4	bS0_IE_BYTE	RW	Data byte transmission complete interrupt enable bit, if the bit is 1, it allows the byte transmission to complete interrupt. If the bit is 0, the interrupt will not be generated when the byte transmission is completed	0
3	bS0_BIT_ORDER	RW	Order control bit of data byte, if the bit is 0, MSB high bit is in front. If the bit is 1, LSB low bit is in front	0
2	Reserved	RO	Reserved	0

1	bS0_SLV_SELT	RO	Chip selection activation status bit in slave mode, if the bit is 0, it indicates not selected currently. If the bit is 1, it indicates being selected currently	0
0	bS0_SLV_PRELOAD	RO	Pre-load data status bit in slave mode, if the bit is 1, it indicates the current pre-load state after the chip selection is valid and before the data has been transmitted	0

SPI0 clock frequency division setting register (SPI0_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_CK_SE	RW	Set SPI0 clock frequency division coefficient in master mode	20h

SPI0 preset data register in slave mode (SPI0_S_PRE)

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_S_PRE	RW	Preload first transmission data in slave mode	20h

SPI0 control register (SPI0_CTRL):

Bit	Name	Access	Description	Reset value
7	bS0_MISO_OE	RW	MISO output enable control bit of SPI0, if the bit is 1, it allows output. If the bit is 0, it disables output	0
6	bS0_MOSI_OE	RW	MOSI output enable control bit of SPI0, if the bit is 1, it allows output. If the bit is 0, it disables output	0
5	bS0_SCK_OE	RW	SCK output enable control bit of SPI0, if the bit is 1, it allows output. If the bit is 0, it disables output	0
4	bS0_DATA_DIR	RW	SPI0 data direction control bit, if the bis 0, the data will be output. Only write FIFO will be regarded as effective operation, and start an SPI transmission. If the bit is 1, the data will be input, write or read FIFO will be regarded as a effective operation, and start an SPI transmission	0
3	bS0_MST_CLK	RW	SPI0 host clock mode control bit, if the bit is 0, the mode will be 0, and the SCK defaults to low level when in idle. If the bit is 1, the mode will be 3, and the SCK defaults to high level	0
2	bS0_2_WIRE	RW	2-line half-duplex mode enable bit of SPI0, if the bit is 0, it will be 3-line full duplex mode, including SCK, MOSI and MISO. If the bit is 1, it will be 2-line half-duplex mode, including SCK, MISO	0
1	bS0_CLR_ALL	RW	If the bit is 1, empty SPI0 interrupt flag and FIFO, and the software is required to reset	1

0	bS0_AUTO_IF	RW	Enable bit that allows automatic reset of byte receiving completion interrupt flag through FIFO effective operation, if the bit is 1, it will automatically reset the byte receiving completion interrupt flag S0_IF_BYTE during the effective read and write operation of FIFO	0

SPI0 data receive/transmit register (SPI0_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_DATA	RW	Including transmit FIFO and receive FIFO physically separated, read operation corresponds to receive data FIFO. Write operation corresponds to transmit data FIFO, and the effective read and write operation can initiate an SPI transmission	xxh

SPI0 state register (SPI0_STAT):

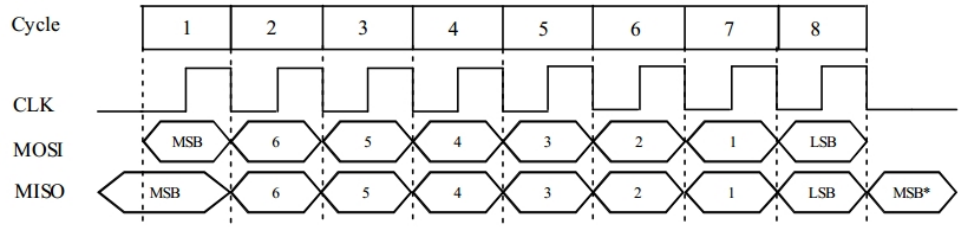
Bit	Name	Access	Description	Reset value
7	S0_FST_ACT	RO	If the bit is 1, it indicates that the current state is the completion of the first byte receiving in slave mode	0
6	S0_IF_OV	RW	FIFO overflow flag bit in slave mode, if the bit is 1, it indicates FIFO overflow interrupt. If the bit is 0, it indicates that there is no interrupt. Direct bit access to reset or write 1 to reset. When bS0_DATA_DIR=0, transmit FIFO empty triggers interrupt. When bS0_DATA_DIR=1, receive FIFO full triggers interrupt	0
5	S0_IF_FIRST	RW	Receive first byte completion interrupt flag bit in slave mode, if the bit is 1, it indicates that the first byte is received. Direct bit access to reset or write 1 to reset	0
4	S0_IF_BYTE	RW	Data byte transmission completon interrupt flag bit, if the bit is 1, it indicates that one byte transmission is completed Direct bit access to reset or write 1 to reset, or reset by FIFO effective operation when bS0_AUTO_IF=1	0
3	S0_FREE	RO	SPI0 idle flag bit, if the bit is 1, it indicates that there is no SPI shift at present, usually it is in the idle period between the data bytes	1
2	S0_T_FIFO	RO	SPI0 transmit FIFO count, effective value is 0 or 1	0
1	Reserved	RO	Reserved	0
0	S0_R_FIFO	RO	SPI0 receive FIFO count, effective value is 0 or 1	0

14.3 SPI Transmission Format

SPI host mode supports two transmission formats, i.e. mode 0 and mode 3. You can select it by setting the

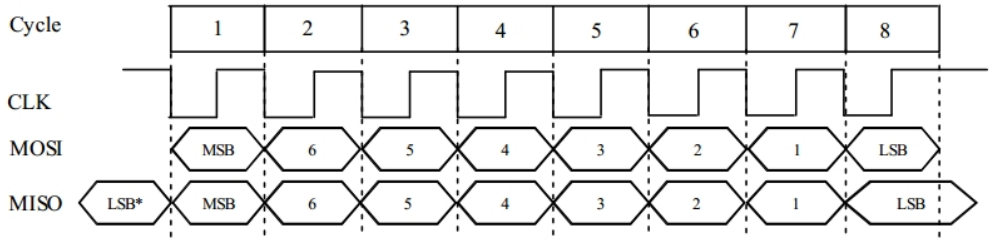
bit bSn_MST_CLK in SPI control register SPIn_CTRL. CH552 always samples MISO data on the rising edge of CLK. The data transmission format is shown in the figure below.

Mode 0: bSn_MST_CLK = 0



Fugure 14.3.1 SPI Mode 0 Sequence Diagram

Mode 3: bSn_MST_CLK = 1



Fugure 14.3.2 SPI Mode 3 Sequence Diagram

14.4 SPI Configuration

14.4.1 SPI Master Mode Configuration

In SPI master mode, SCK pin output serial clock, and chip selection output pins can be specified as any I/O pins.

SPI0 configuration steps:

(1) Set SPI clock frequency division setting register SPI0_CK_SE, and configure SPI clock frequency.

(2). Set the bit bS0_MODE_SLV of SPI setting register SPI0_SETUP to 0, and configure as the master mode.

(3). Set the bit bS0_MST_CLK of SPI control register SPI0_CTRL, and set as mode 0 or 3 as required.

(4). Set the bit bS0_SCK_OE and bS0_MOSI_OE of SPI control register SPI0_CTRL to 1, and the bit bS0_MISO_OE to 0, set the P1 port direction bSCK and bMOSI as output, bMISO as input, and chip selection pin as output.

Data transmission process:

(1). Write SPI0_DATA register, write the data to be sent to FIFO to automatically initiate an SPI transmission.

(2). Wait for S0_FREE to be 1, it indicates that the transmission is completed and the transmission of the next byte can be proceeded.

Data reception process:

(1). Write SPI0_DATA register, write any data to FIFO, e.g. 0FFh, to initiate an SPI transmission.

(2). Wait for S0_FREE to be 1, it indicates that the reception is completed and can read SPI0_DATA to obtain the received data.

(3). If bS0_DATA_DIR is set to 1 previously, the above read operation will also initiate the next SPI

transmission, otherwise it will not start.

14.4.2 SPI Slave Mode Configuration

Only SPI0 supports the slave mode. In the slave mode, SCK pin is used to receive the serial clock of the connected SPI host.

(1). Set the bit bS0_MODE_SLV of SPI0 setting register SPI0_SETUP to 1, and configure as the slave mode.

(2). Set the bit bS0_SCK_OE and bS0_MOSI_OE of SPI0 control register SPI0_CTRL to 0, and the bit bS0_MISO_OE to 1, set the P1 port direction bSCK, bMOSI and bMISO as well as chip selection pin as input. When SCS chip selection is valid (low level), MISO will automatically enable output. At the same time, it is recommended to set MISO pin as high impedance input mode (P1_MOD_OC[6]=0, P1_DIR_PU[6]=0), so that MISO will not output during invalid chip selection, which is convenient for sharing SPI bus.

(3). Optionally, set the preset data register SPI0_S_PRE in SPI slave mode, to be automatically loaded into the buffer for the first time after chip selection for external output. After 8 serial clocks, that is, the first byte of data transmission and exchange is completed, CH552 obtains the first byte of data (possibly command code) sent by the external SPI host, and the external SPI host obtains the preset data (possibly the status value) in SPI0_S_PRE through exchange. The bit 7 of register SPI0_S_PRE will be automatically loaded into the MISO pins during the low level period of SCK after the SPI chip selection is effective. For SPI mode 0, if the bit 7 of SPI0_S_PRE is preset by CH552, the external SPI host will obtain the preset value of bit 7 of SPI0_S_PRE by inquiring the MISO pins when the SPI chip selection is effective but has no data transmission, thereby the value of bit 7 of SPI0_S_PRE can be obtained only by the effective SPI chip selection.

Data transmission process:

Inquire S0_IF_BYTE or wait for interrupt, and after each SPI data byte transmission, write the SPI0_DATA register and write the data to be sent to FIFO. Or wait for S0_FREE to be changed from 0 to 1, and the transmission of the next byte can be proceeded.

Data reception process:

Inquire S0_IF_BYTE or wait for interrupt, and after each SPI data byte transmission, read the SPI0_DATA register and obtain the received data from FIFO. Inquire S0 R FIFO to know whether there are any remaining bytes in the FIFO.

15. Analog-to-Digital Converter (ADC) and Voltage Comparator (not apply to CH551)

15.1 ADC Introduction

CH552 chip provides an 8-bit analog digital converter, including voltage comparator and ADC module. The converter has 4 analog signal input channels, which allows time-sharing acquisition, and supports analog input voltage that ranges from 0 to VCC.

15.2 ADC Register

Table 15.2.1 List of ADC Related Register

Name	Address	Description	Reset

			value
ADC_CTRL	80h	ADC control register	x0h
ADC_CFG	9AH	ADC configuration register	00h
ADC_DATA	9Fh	ADC data register	xxh

ADC control register (ADC_CTRL):

Bit	Name	Access	Description	Reset value
7	CMPO	RO	The result output bit of the voltage comparator, if the bit is 0, it indicates that the voltage of the positive phase input terminal is lower than that of the inverting input terminal. If the bit is 1, it indicates that the voltage of the positive phase input terminal is higher than that of the inverted input terminal	x
6	CMP_IF	RW	Voltage comparator result change flag, if the bit is 1, it indicates that the voltage comparator results have changed, and the direct bit access reset to zero	0
5	ADC_IF	RW	ADC conversion completion interrupt flag, if the bit is 1, it indicates that an ADC conversion is completed, and the direct bit access reset to zero	0
4	ADC_START	RW	ADC start control bit, set 1 to start an ADC conversion, the bit will be reset automatically after the ADC conversion is completed	0
3	CMP_CHAN	RW	Voltage comparator inverted input terminal selection: 0-AIN1; 1-AIN3	0
2	Reserved	RO	Reserved	0
1	ADC_CHAN1	RW	High bit is selected for the voltage comparator positive phase input terminal and ADC input channel	0
0	ADC_CHAN0	RW	Low bit is selected for the voltage comparator positive phase input terminal and ADC input channel	0

Table 15.2.1 Voltage Comparator CMP Positive Phase Input Terminal and ADC Input Channel Table

ADC_CHAN1	ADC_CHAN0	Select the voltage comparator positive phase input terminal and ADC input channel
0	0	AIN0 (P1.1)
0	1	AIN1 (P1.4)
1	0	AIN2 (P1.5)
1	1	AIN3 (P3.2)

ADC configuration register (ADC_CFG):

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0000b
3	ADC_EN	RW	The power control bit of ADC module, if the bit is 0, it	0

			indicates that turn off the power supply of the ADC module and enter the sleep state. If the bit is 1, it indicates ON	
2	CMP_EN	RW	The power control bit of voltage comparator, if the bit is 0, it indicates that turn off the power supply of the voltage comparator and enter the sleep state. If the bit is 1, it indicates ON	0
1	Reserved	RO	Reserved	0
0	ADC_CLK	RW	ADC reference clock frequency selection bit, if the bit is 0, select the slow clock, and 384 Fosc cycles are required for each ADC. If the bit is 1, select the fast clock, and 96 Fosc cycles are required for each ADC	0

ADC data register (ADC_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_DATA	RO	ADC sampling result data	xxh

15.3 ADC Function

ADC sampling mode configuration steps:

(1). Set the ADC_EN bit in ADC_CFG register as 1, turn on ADC module, and set the bADC_CLK to select frequency.

(2). Set ADC_CHAN1/0 in ADC_CTRL register, and select the input channel.

(3). Optional, reset interrupt flag ADC_IF. Optional, if the interrupt mode is used, the interrupt needs to be enabled here.

(4). Set ADC_START in ADC_CTRL register, and start an ADC conversion.

(5). Wait for ADC_START to be changed into 0, or ADC_IF to be set to 1 (if reset to zero before), it indicates that the result data can be read through ADC_DATA after ADC conversion. This data is the value of the input voltage relative to 255 equal parts of the VCC supply voltage, for example, if the result data is 47, it indicates that the input voltage is approximate to 47/255 of the VCC voltage. If the VCC supply voltage is also uncertain, another determined reference voltage value can be measured, and the measured input voltage value and the VCC supply voltage value can be calculated proportionally.

(6). If ADC_START is set again, start the next ADC conversion.

Voltage comparator mode configuration steps:

(1). Set the CMP_EN bit in ADC_CFG register as 1, turn on the voltage comparator module.

(2). Set ADC_CHAN1/0 and CMP_CHAN in ADC_CTRL register, and select the positive and inverted input channels.

(3). Optional, reset flag CMP_IF.

(4). You can inquire the status of the CMPO bit at any time to obtain the results of the current comparator.

(5). If the CMP_IF is changed into 1, it indicates that the result of the comparator has changed.

For the above selected analog signal input channel, the GPIO pin where it's located must be set in either high-impedance input mode or open-drain output mode and in output 1 state (equivalent to high-impedance

input), Pn_DIR_PU[x]=0, and it is recommended to turn off the pull-up resistor and pull-down resistor.

16. USB Controller

16.1 USB Controller Introduction

CH552 is built-in with USB controller and USB transceiver, with the features as follows:

(1). Support USB Device function, support USB 2.0 full speed 12Mbps or low speed 1.5Mbps;

(2). Support USB control transmission, bulk transmission, interrupt transmission, synchronous/real-time transmission;

(3). Support data packet of up to 64 bytes, built-in FIFO, support interrupts and DMA.

The USB related registers of CH552 are divided into 2 parts: USB global register and USB endpoint register.

16.2 Global Register

Table 16.2.1 USB Global Register List (those marked in grey are controlled by bUC_RESET_SIE reset)

Name	Address	Description	Reset value
USB_C_CTRL	91h	USB type-C configuration channel control register	0000 0000b
USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
USB_INT_ST	D9h	USB interrupt status register (read only)	00xx xxxxb
USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
USB_RX_LEN	DBh	USB receive length register (read only)	0xxx xxxxb
USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
USB_CTRL	E2h	USB control register	0000 0110b
USB_DEV_AD	E3h	USB device address register	0000 0000b

USB type-C configuration channel control register (USB_C_CTRL): (not apply to CH551)

Bit	Name	Access	Description	Reset value
7	bVBUS2_PD_EN	RW	If the bit is 1, enable the internal 10K pull-down resistor of VBUS2 pin. If the bit is 0, disable.	0
6	bUCC2_PD_EN	RW	If the bit is 1, enable the internal 5.1K pull-down resistor of UCC2 pin. If the bit is 0, disable.	0
5	bUCC2_PU1_EN	RW	This bit is the high bit of the internal pull-up resistor control selection of UCC2 pin	0
4	bUCC2_PU0_EN	RW	This bit is the low bit of the internal pull-up resistor control selection of UCC2 pin	0
3	bVBUS1_PD_EN	RW	If the bit is 1, enable the internal 10K pull-down resistor of VBUS1 pin. If the bit is 0, disable.	0
2	bUCC1_PD_EN	RW	If the bit is 1, enable the internal 5.1K pull-down resistor of UCC1 pin. If the bit is 0, disable.	0
1	bUCC1_PU1_EN	RW	This bit is the high bit of the internal pull-up resistor control selection of UCC1 pin	0
0	bUCC1_PU0_EN	RW	This bit is the low bit of the internal pull-up resistor	0

			control selection of UCC1 pin	

The pull-up resistor inside the UCCn pin is selected by bUCCn_PU1_EN and bUCCn_PU0_EN.

bUCCn_PU1_EN	bUCCn_PU0_EN	Select the pull-up resistor inside the UCCn pin
0	0	Disable the internal pull-up resistor
0	1	Enable internal 56KΩ pull-up resistor, it indicates providing default USB current
1	0	Enable internal 22KΩ pull-up resistor, it indicates providing 1.5A current
1	1	Enable internal 10KΩ pull-up resistor, it indicates providing 3A current

The above mentioned USB type - C pull-up resistor and pull-down resistor are independent from the Pn_DIR_PU port direction control and the port pull-up resistor controlled by the pull-up enable register, when a pin is used for USB type-C, the corresponding port pull-up resistor of the pin should be forbidden. It's recommended to enable the high impedance input mode of the pin (to avoid low level or high level output by the pin).

For detailed control and input detection of USB type-C configuration channels, please refer to USB type-C application commands and routines.

USB interrupt flag register (USB_INT_FG):

Bit	Name	Access	Description	Reset value
7	U_IS_NAK	RO	If the bit is 1, it indicates that NAK busy response is received during current USB transmission. If the bit is 0, it indicates that non-NAK response is received	0
6	U_TOG_OK	RO	Current USB transmission DATA0/1 synchronization flag matching state, if the bit is 1, it indicates synchronization and the data is valid. If the bit is 0, it indicates desynchrony and the data may be invalid	0
5	U_SIE_FREE	RO	Idle status bit of USB protocol processor, if the bit is 0, it indicates busy and USB transmission is in progress. If the bit is 1, it indicates USB in idle	1
4	UIF_FIFO_OV	RW	USB FIFO overflow interrupt flag bit, if the bit is 1, it indicates FIFO overflow interrupt. If the bit is 0, it indicates that there is no interrupt. Direct bit access to reset or write 1 to reset	0
3	Reserved	RO	Reserved	0
2	UIF_SUSPEND	RW	USB bus suspended or wake-up event interrupt flag bit, if the bit is 1, it indicates that there is an interrupt, and the interrupt is triggered by USB suspended event or wake-up event. If the bit is 0, it indicates that there is no interrupt. Direct bit access to reset or write 1 to reset	0
1	UIF_TRANSFER	RW	USB transmission completion interrupt flag bit, if the bit is 1, it indicates that there is an interrupt, and the	0

			interrupt is triggered by a USB transmission completion. If the bit is 0, it indicates that there is no interrupt. Direct bit access to reset or write 1 to reset	
0	UIF_BUS_RST	RW	USB bus reset event interrupt flag bit, if the bit is 1, it indicates that there is an interrupt, and the interrupt is triggered by the USB bus reset event. If the bit is 0, it indicates that there is no interrupt. Direct bit access to reset or write 1 to reset	0

USB interrupt state register (USB_INT_ST):

Bit	Name	Access	Description	Reset value
7	bUIS_IS_NAK	RO	If the bit is 1, it indicates that NAK busy response is received during current USB transmission. The same as U_IS_NAK	0
6	bUIS_TOG_OK	RO	Current USB transmission DATA0/1 synchronization flag matching state, if the bit is 1, it indicates synchronization. If the bit is 0, it indicates desynchrony. The same as U_TOG_OK	0
5	bUIS_TOKEN1	RO	The token PID high bit of the current USB transmission service	x
4	bUIS_TOKEN0	RO	The token PID low bit of the current USB transmission service	x
[3:0]	MASK_UIS_ENDP	RO	The endpoint number of the current USB transmission service, 0000 represents endpoint 0; ...; 1111 represents endpoint 15	xxxxb

BUIS_TOKEN1 and bUIS_TOKEN0 constitute MASK_UIS_TOKEN, which is used to identify the token PID of the current USB transmission service: 00 represents OUT package; 01 represents SOF package; 10 represents IN package; 11 represents SETUP package.

USB miscellaneous state register (USB_MIS_ST):

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	Reserved	xxb
5	bUMS_SIE_FREE	RO	Idle status bit of USB protocol processor, if the bit is 0, it indicates busy and USB transmission is in progress. If the bit is 1, it indicates USB in idle. The same as U_SIE_FREE	1
4	bUMS_R_FIFO_RDY	RO	USB receive FIFO data ready status bit, if the bit is 0, it indicates that receive FIFO is null. If the bit is 1, it indicates that receive FIFO is not null	0
3	bUMS_BUS_RESET	RO	USB bus reset status bit, if the bit is 0, it indicates that there is no USB bus reset at present. If the bit is 1, it indicates that USB bus reset is in progress	1

2	bUMS_SUSPEND	RO	USB suspending status bit, if the bit is 0, it indicates that there is USB activity at present. If the bit is 1, it indicates that there has been no USB activity for some time and suspending is requested	0
[1:0]	Reserved	RO	Reserved	00b

USB receive length register (USB_RX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes of the data received by the current USB endpoint	xxh

USB interrupt enable register (USB_INT_EN):

Bit	Name	Access	Description	Reset value
7	bUIE_DEV_SOF	RW	If the bit is 1, enable receiving SOF package interrupt. If the bit is 0, disable.	0
6	bUIE_DEV_NAK	RW	If the bit is 1, enable receiving NAK interrupt. If the bit is 0, disable.	0
5	Reserved	RO	Reserved	0
4	bUIE_FIFO_OV	RW	If the bit is 1, enable FIFO overflow interrupt. If the bit is 0, close enable	0
3	Reserved	RO	Reserved	0
2	bUIE_SUSPEND	RW	If the bit is 1, enable USB bus suspended or wake-up event interrupt. If the bit is 0, disable.	0
1	bUIE_TRANSFER	RW	If the bit is 1, enable USB transmission completion interrupt. If the bit is 0, disable.	0
0	bUIE_BUS_RST	RW	If the bit is 1, enable USB bus reset event interrupt. If the bit is 0, disable.	0

USB control register (USB_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUC_LOW_SPEED	RW	USB bus signal transmission rate selection bit, if the bit is 0, select full speed 12Mbps. If the bit is 1, select low speed 1.5Mbps	0
5	bUC_DEV_PU_EN	RW	USB device enable and internal pull-up resistor control bit. if the bit is 1, enable USB device transmission and enable internal pull-up resistor	0
5	bUC_SYS_CTRL1	RW	USB system control high bit	0
4	bUC_SYS_CTRL0	RW	USB system control low bit	0
3	bUC_INT_BUSY	RW	Automatical pause enable bit before the USB transmission completion interrupt flag is not reset, if the	0

			bit is 1, it will automatically pause and reply to the busy NAK before the interrupt flag UIF_TRANSFER is reset. If the bit is 0, it will not pause	
2	bUC_RESET_SIE	RW	USB protocol processor software reset control bit, if the bit 1, it will forcefully reset the USB protocol processor and most of the USB control registers, which requires the software to reset	1
1	bUC_CLR_ALL	RW	If the bit is 1, empty USB interrupt flag and FIFO, which requires the software to reset	1
0	bUC_DMA_EN	RW	If the bit is 1, enable USB DMA and DMA interrupt. If the bit is 0, close enable	0

bUC_SYS_CTRL1 and bUC_SYS_CTRL0 constitute the USB system control combination:

bUC_SYS_CTRL1	bUC_SYS_CTRL0	USB system control description
0	0	Disable USB device function, turn off internal pull-up resistor
0	1	Enable USB device function, turn off internal pull-up, and external pull-up is required.
1	X	Enable USB device function, turn on internal 1.5KΩ pull-up resistor This pull-up resistor is prior to the pull-down resistor, which also can be used in GPIO mode

USB device address register (USB_DEV_AD):

Bit	Name	Access	Description	Reset value
7	bUDA_GP_BIT	RW	USB common flag bit, user-defind, and reset or set by software	0
[6:0]	MASK_USB_ADDR	RW	Address of the USB device	00h

16.3 Endpoint Register

CH552 provides 5 sets of bidirectional endpoints, including endpoint0, endpoint1, endpoint2, endpoint3 and endpoint4. The maximum data packet length of all endpoints is 64 bytes.

Endpoint0 is the default endpoint and supports control transmission. The transmit endpoint and receive endpoint share a 64-byte data buffer area.

Endpoint1, endpoint2, endpoint3 each includes a transmit endpoint IN and a receive endpoint OUT. The transmit endpoint and receive endpoint each has a separate 64 bytes or double 64 bytes data buffer respectively, supporting control transmission, bulk transmission, interrupt transmission, and real-time/synchronous transmission.

Endpoint4 each includes a transmit endpoint IN and a receive endpoint OUT. The transmit endpoint and receive endpoint each has a separate 64 bytes data buffer respectively, supporting control transmission, bulk transmission, interrupt transmission, and real-time/synchronous transmission.

Each group of endpoints has a control register UEPn_CTRL and a length transmit register UEPn_T_LEN(n=0/1/2/3/4), which are used to set the synchronization trigger bit of endpoint, the response

to OUT transactions and IN transactions and the length of data to be sent.

As the necessary USB bus pull-up resistor of USB device, it can be set whether to be enabled by the software at any time. When bUC_DEV_PU_EN in the USB control register USB_CTRL is set to 1, CH552 will internally connect the pull-up resistor with the DP pin or DM pin of the USB bus based on bUD_LOW_SPEED and enable the USB device function.

When a USB bus reset, USB bus suspended or wake-up event is detected, or when the USB successfully processes data transmission or reception, the USB protocol processor will set corresponding interrupt flag and generate an interrupt request. The application program can directly query, or query and analyze the interrupt flag register USB_INT_FG in the USB interrupt service program, and perform corresponding processing according to UIF_BUS_RST and UIF_SUSPEND. In addition, if UIF_TRANSFER is valid, it is required to continue to analyze the USB interrupt state register USB_INT_ST, and perform the corresponding processing according to the current endpoint number MASK_UIS_ENDP and the current transaction token PID identifier MASK_UIS_TOKEN. If the synchronization trigger bit bUEP_R_TOG of OUT transaction of each endpoint is set in advance, you can judge whether the synchronization trigger bit of the data packet received matches the synchronization trigger bit of the endpoint through U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid. If the data is not synchronized, the data should be discarded. After the USB transmit or receive interrupt is processed each time, the synchronization trigger bit of corresponding endpoint should be modified correctly to synchronize the data packet sent next time and detect whether the data packet received next time is synchronized. In addition, bUEP_AUTO_TOG can be set to automatically flip the corresponding synchronization trigger bit after successful transmission oe reception.

The data to be transmissted by each endpoint is in their own buffer, and the length of the data to betransmitted is independently set in UEPn_T_LEN. The data received by each endpoint is in their own buffer, but the length of the data received is in the USB receive length register USB_RX_LEN, and it can be distinguished according to the current endpoint number when the USB is receiving an interrupt.

Table 16.3.1 List of USB Device Endpoint Related Registers (those marked in grey are controlled by RB_UC_RESET_SIE reset)

Name	Address	Description	Reset value
UDEV_CTRL	D1h	USB device physical port control register	10xx 0000b
UEP1_CTRL	D2h	Endpoint1 control register	0000 0000b
UEP1_T_LEN	D3h	Endpoint1 transmist length register	0xxx xxxxb
UEP2_CTRL	D4h	Endpoint2 control register	0000 0000b
UEP2_T_LEN	D5h	Endpoint2 transmist length register	0000 0000b
UEP3_CTRL	D6h	Endpoint3 control register	0000 0000b
UEP3_T_LEN	D7h	Endpoint3 transmist length register	0xxx xxxxb
UEP0_CTRL	DCh	Endpoint0 control register	0000 0000b
UEP0_T_LEN	DDh	Endpoint0 transmist length register	0xxx xxxxb
UEP4_CTRL	DEh	Endpoint4 control register	0000 0000b
UEP4_T_LEN	DFh	Endpoint4 transmist length register	0xxx xxxxb
UEP4_1_MOD	EAh	Endpoint1, endpoint4 mode control register	0000 0000b
UEP2_3_MOD	EBh	Endpoint2, endpoint3 mode control register	0000 0000b
UEP0_DMA_H	EDh	Endpoint0 and endpoint4 buffer start address high byte	0000 00xxb
UEP0_DMA_L	ECh	Endpoint0 and endpoint4 buffer start address low byte	xxxx xxxxb

UEP0_DMA	ECh	UEP0_DMA_L and UEP0_DMA_H constitute a 16-bit SFR	0xxxh
UEP1_DMA_H	EFh	Endpoint1 buffer area start address high byte	0000 00xxb
UEP1_DMA_L	EEh	Endpoint1 buffer area start address low byte	xxxx xxxxb
UEP1_DMA	EEh	UEP1_DMA_L and UEP1_DMA_H constitute a 16-bit SFR	0xxxh
UEP2_DMA_H	E5h	Endpoint2 buffer area start address high byte	0000 00xxb
UEP2_DMA_L	E4h	Endpoint2 buffer area start address low byte	xxxx xxxxb
UEP2_DMA	E4h	UEP2_DMA_L and UEP2_DMA_H constitute a 16-bit SFR	0xxxh
UEP3_DMA_H	E7h	Endpoint3 buffer area start address high byte	0000 00xxb
UEP3_DMA_L	E6h	Endpoint3 buffer area start address low byte	xxxx xxxxb
UEP3_DMA	E6h	UEP3_DMA_L and UEP3_DMA_H constitute a 16-bit SFR	0xxxh

USB device physical port control register (UDEV_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
7	bUD_PD_DIS	RW	USB device port UDP/UDM pin internal pull-down resistor disable bit, if the bit is 1, disable the internal pull-down resistor. If the bit is 0, enable the internal pull-down resistor. This bit is not controlled by bUSB_IO_EN, and it also can be used in GPIO mode to provide pull-down resistor	1
6	Reserved	RO	Reserved	0
5	bUD_DP_PIN	RO	Current UDP pin status 0 represents low level; 1 represents high level	x
4	bUD_DM_PIN	RO	Current UDM pin status 0 represents low level; 1 represents high level	x
3	Reserved	RO	Reserved	0
2	bUD_LOW_SPEED	RW	USB device physical port low speed mode enable bit, if the bit is 1, select 1.5Mbps low speed mode. If the bit is 0, select 12Mbps full speed mode	0
1	bUD_GP_BIT	RW	Device common flag bit, user-defines, and reset or set by software	0
0	bUD_PORT_EN	RW	USB device physical port enable bit, if the bit is 1, enable physical port. If the bit is 0, disable the physical port	0

Endpoint n control register (UEPn_CTRL):

Bit	Name	Access	Description	Reset value
7	bUEP_R_TOG	RW	The synchronization trigger bit expected by the receiver of USB endpoint n (handle SETUP/OUT services). If the bit is 0, expected DATA0. If the bit is 1, expected DATA1	0
6	bUEP_T_TOG	RW	The synchronization trigger bit prepared by the transmitter of USB endpoint n (handle IN services). If	0

			the bit is 0, transmit DATA0. If the bit is 1, transmit DATA1.	
5	Reserved	RO	Reserved	0
4	bUEP_AUTO_TOG	RW	The synchronization trigger bit automatic turnover enable control bit. If the bit is 1, automatic turnonver of the corresponding synchronization trigger bit after sucessful transmission or reception. If the bit is 0, no automatic turnover, but manual switch is allowed. Only support endpoint1/2/3	0
3	bUEP_R_RES1	RW	Response control high bit from the receiver of endpoint n to SETUP/OUT services	0
2	bUEP_R_RES0	RW	Response control low bit from the receiver of endpoint n to SETUP/OUT services	0
1	bUEP_T_RES1	RW	Response control high bit from the transmitter of endpoint n to IN services	0
0	bUEP_T_RES0	RW	Response control low bit from the transmitter of endpoint n to IN services	0

MASK_UEP_R_RES, consisting of bUEP_R_RES1 and bUEP_R_RES0, is used to control the response of the receiver of endpoint n to the SETUP/OUT services: 00 represents reply ACK or ready. 01 represents timeout/no response, which is used to realize real-time/synchronous transmission of non-endpoint0. 10 represents reply NAK or busy. 11 represents reply STALL or error.

MASK_UEP_T_RES, consisting of bUEP_T_RES1 and bUEP_T_RES0, is used to control the response of the transmitter of endpoint n to the IN services: 00 represents reply DATA0/DATA1 or data ready or expected ACK. 01 represents reply DATA0/DATA1 and expected no response, which is used to realize real-time/synchronous transmission of non-endpoint0. 10 represents reply NAK or busy. 11 represents reply STALL or error.

Endpoint n transmit length register (UEPn_T_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUEPn_T_LEN	RW	Set the number of data bytes that USB endpointn (n=0/1/3/4) is ready to send	xxh
	bUEP2_T_LEN		Set the number of data bytes that USB endpoint2 is ready to send	00h

USB endpoint1, endpoint4 mode control register (UEP4_1_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP1_RX_EN	RW	If the bit is 0, it represents disable receiving by endpoint1. If the bit is 1, it represents enable receiving by endpoint1 (OUT)	0
6	bUEP1_TX_EN	RW	If the bit is 0, it represents disable sending by endpoint1. If the bit is 1, it represents enable sending by endpoint 1 (IN)	0

5	Reserved	RO	Reserved	0
4	bUEP1_BUF_MOD	RW	Endpoint 1 data buffer mode contro bit	0
3	bUEP4_RX_EN	RO	If the bit is 0, it represents disable receiving by endpoint4. If the bit is 1, it represents enable receiving by endpoint4 (OUT)	0
2	bUEP4_TX_EN	RW	If the bit is 0, it represents disable sending by endpoint4. If the bit is 1, it represents enable sending by endpoint4 (IN)	0
[1:0]	Reserved	RO	Reserved	00b

The data buffer modes of USB endpoint0 and endpoint4 are controlled by a combination of bUEP4_RX_EN and bUEP4_TX_EN, refer to the following table.

Table 16.3.2 Endpoint0 and endpoint4 Buffer Mode

bUEP4_RX_EN	bUEP4_TX_EN	Structure description: arrange from low to high with UEP0 DMA as the start address
0	0	Endpoint0 single 64-byte receive/transmit shared buffers (IN and OUT)
1	0	Endpoint0 single 64-byte receive/transmit shared buffers. Endpoint4 single 64-byte receive buffer (OUT)
0	1	Endpoint0 single 64-byte receive/transmit shared buffers. Endpoint4 single 64-byte transmit buffer (IN)
1	1	Endpoint0 single 64-byte receive/transmit shared buffers. Endpoint4 single 64-byte receive buffer (OUT). Endpoint4 single 64-byte transmit buffer (IN). All 192 bytes are arranged as follows: UEP0_DMA+0 address: endpoint0 receive/transmit; UEP0_DMA+64 address: endpoint4 receive; UEP0_DMA+128: endpoint4 transmit

USB endpoint2, endpoint3 mode control register (UEP2_3_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP3_RX_EN	RW	If the bit is 0, disable receiving by endpoint3. If the bit is 1, enable receiving by endpoint3 (OUT)	0
6	bUEP3_TX_EN	RW	If the bit is 0, disable sending by endpoint3. If the bit is 1, enable sending by endpoint3 (IN)	0
5	Reserved	RO	Reserved	0
4	bUEP3_BUF_MOD	RW	Endpoint3 data buffer mode control bit	0
3	bUEP2_RX_EN	RO	If the bit is 0, disable receiving by endpoint2. If the bit is 1, enable receiving by endpoint2 (OUT)	0
2	bUEP2_TX_EN	RW	If the bit is 0, disable sending by endpoint2. If the bit is 1, enable sending by endpoint2 (IN)	0
1	Reserved	RO	Reserved	0
0	bUEP2_BUF_MOD	RW	Endpoint2 data buffer mode contro bit	0

The data buffer modes of USB endpoint1, endpoint2 and endpoint3 are controlled by a combination of bUEPn_RX_EN, bUEPn_TX_EN and bUEPn_BUF_MOD(n=1/2/3) respectively, refer to the following

table. In the double-64 byte buffer mode, the first 64-byte buffer will be selected based on bUEP_*_TOG=0 and the last 64-byte buffer will be selected based on bUEP_*_TOG=1 during USB data transmission to realize automatic switch.

Table 16.3.3 Endpointn (n=1/2/3) Buffer Mode

bUEPn_RX_EN	bUEPn_TX_EN	bUEPn_BUF_MOD	Structure description: arrange from low to high with UEPn_DMA as the start address
0	0	x	Endpoint is disabled, and the UEPn_DMA buffer is not used
1	0	0	Single-64-byte receive buffer (OUT)
1	0	1	Double 64-byte receive buffer, selected by bUEP_R_TOG.
0	1	0	Single-64-byte transmit buffer (IN)
0	1	1	Double-64-byte transmit buffer, selected by bUEP_T_TOG.
1	1	0	Single-64-byte receive buffer (OUT). Single 64-byte transmit buffer (IN)
1	1	1	Double-64-byte receive buffer, selected by bUEP_R_TOG. Double 64-byte transmit buffer, selected by bUEP_T_TOG. All 256 bytes are arranged as follows: UEPn_DMA+0 address: endpoint reception when bUEP_R_TOG=0; UEPn_DMA+64 address: endpoint reception when bUEP_R_TOG=1; UEPn_DMA+128 address: endpoint transmission when bUEP_T_TOG=0; UEPn_DMA+192 address: endpoint transmission when bUEP_T_TOG=1

USB endpointn (n=0/1/2/3) buffer start address (UEPn_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	UEPn_DMA_H	RW	Endpointn buffer start address high byte, only the lower 2 bits are valid, and the higher 6 bits are fixed to be 0	0xh
[7:0]	UEPn_DMA_L	RW	Endpointn buffer area start address low byte	xxh

Note: the length of the buffer that receives data >= min (maximum data packet length possibly received + 2 bytes, 64 bytes)

17. Touch-Key

17.1 Touch-Key Introduction

CH552 chip provides capacitance detection module and related timer. It has 6 input channels and supports capacitance range of 5pF~150pF. Self-capacitance mode can support up to 6 touch keys, while mutual capacitance mode can support up to 15 touch keys.

17.2 Touch-Key Register

Table 17.2.1 List of Touch-Key Related Registers

Name	Address	Description	Reset value
TKEY_CTRL	C3h	Touch-Key control register	x0h
TKEY_DATH	C5h	Touch-Key data high byte (read only)	00h
TKEY_DATL	C4h	Touch-Key data low byte (read only)	xxh
TKEY_DAT	C4h	TKEY_DATL and KEY_DATH constitute a 16-bit SFR	00xxh

Touch-Key control register (TKEY_CTRL):

Bit	Name	Access	Description	Reset value
7	bTKC_IF	RO	Timing interrupt flag. If bTKD_CHG=0, it will automatically set to 1 and request interrupt at the end of the current timing cycle, and it will automatically reset to zero at the end of the preparation stage, or reset to zero by writing TKEY_CTRL. If bTKD_CHG=1, it will automatically reset to zero and request no interrupt, skip the current cyle, and then re-prepare and detect in the next cycle, and automatically set to 1 and request for interrupt at the end of the next cycle	x
[6:5]	Reserved	RO	Reserved	00b
4	bTKC_2MS	RW	Cycle selection of capacitance detection timer: 0~1mS; 1~2 mS. The first 87uS of each cycle is for preparation, and the remaining time is for detection. The above time is based on the time when Fosc=24MHz	0
3	Reserved	RO	Reserved	0
2	bTKC_CHAN2	RW	Touch key capacitance detection input selection high bit	0
1	bTKC_CHAN1	RW	Touch key capacitance detection input selection median bit	0
0	bTKC_CHAN0	RW	Touch key capacitance detection input selection low bit	0

The input channel of touch key capacitance detection is selected by bTKC_CHAN2~bTKC_CHAN0.

bTKC_CHAN2	bTKC_CHAN1	bTKC_CHAN0	Select touch key capacitance detection input channel
0	0	0	Turn off the power of capacitance detection module, Only used for independent timing interrupts with cycles of 1mS or 2mS
0	0	1	TIN0 (P1.0)
0	1	0	TIN1 (P1.1)
0	1	1	TIN2 (P1.4)
1	0	0	TIN3 (P1.5)
1	0	1	TIN4 (P1.6)

1	1	0	TIN5 (P1.7)
1	1	1	Turn on the power of capacitance detection module without connecting any channel

Touch-Key data register (TKEY_DAT):

Bit	Name	Access	Description	Reset value
7	bTKD_CHG TKEY_DATH[7]	RO	Touch-Key control change flag. If the bit is 1, TKEY_CTRL is rewritten during capacitance detection, which may result in invalid TKEY_DAT data, and bTKC_IF will not be set at the end of the current cycle. The bit is automatically reset at the end of the preparation stage of each timing cycle, and the bit should be shielded to obtain the data	0
6	Reserved	RO	Reserved	0
[5:0]	TKEY_DATH	RO	Touch-Key data high byte. Automatic reset at the end of the preparation stage of each timing cycle. Automatic counting in the capacitance detection stage. Keep the data unchanged in the preparation stage to read the timing interrupt program	00h
[7:0]	TKEY_DATL	RO	Touch-Key data low byte. Automatic reset at the end of the preparation stage of each timing cycle. Automatic counting in the capacitance detection stage. Keep the data unchanged in the preparation stage to read the timing interrupt program	xxh

17.3 Touch-Key Function

Capacitance detection steps:

(1). Set bTKC_2MS and bTKC_CHAN2 ~ bTKC_CHAN0 in the TKEY_CTRL register, select the cycle and input channel. For the selected input channel, the GPIO pin where it's located must be set in either high-impedance input mode or open-drain output mode and in output 1 state (equivalent to high-impedance input), Pn_DIR_PU[x]=0.

(2). Reset bTKC_IF and turn on interrupt IE_TKEY to wait for timing interrupt, or enter the interrupt program by actively querying bTKC_IF.

(3). Upon the completion of the capacitance detection of the current channel, bTKC_IF request interrupt will be set automatically, meanwhile enter the preparation stage of the next cycle, and keep the TKEY_DAT data unchanged about 87uS.

(4). Enter the interrupt program, firstly read the capacitance data of the current channel from TKEY_DAT, and shield the highest bit bTKD_CHG. This data is the relative value which is inversely proportional to the capacitance. When the touch key is pressed, the data is smaller than that when the key is not pressed.

(5). Set bTKC_2MS and bTKC_CHAN2 ~ bTKC_CHAN0 in TKEY_CTRL register, and select the next input channel. This write operation will automatically reset bTKC_IF, and end the interrupt request.

(6). The TKEY_DAT data read in step (4) is compared with that saved before when there is no pressing of the key to determine whether there is capacitance change and whether any key is pressed.

(7). Interrupt returns, and then turn to step (3) after the capacitance detection of the next channel is completed.

18. Parameters

18.1 Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description	Min.	Max.	Unit
TA	Ambient temperature during operation	-40	85	℃
TS	Ambient temperature during storage	-55	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.4	5.8	V
VIO	Voltage on other input or output pins except for P3.6/P3.7	-0.4	VCC+0.4	V
VIOU	Voltage on P3.6/P3.7 input or output pins	-0.4	V33+0.4	V

18.2 Electrical Parameters at 5V

Test Conditions: TA=25℃, VCC=5V, Fsys=6MHz

Name	Parameter description		Min.	Typ.	Max.	Unit
VCC5	VCC pin supply voltage	V33 only connects with an external capacitor	3.7	5	5.5	V
V33	Internal USB power regulator output voltage		3.14	3.27	3.4	V
ICC24M5	Total supply current during operation at Fsys=24MHz		8	11		mA
ICC6M5	Total supply current during operation at Fsys=6MHz		4	6		mA
ICC750K5	Total supply current during operation at Fsys=750KHz		2	3		mA
ISLP5	Total supply current after sleep			0.1	0.2	mA
ISLP5L	Total supply current when VCC=V33=5V, external crystal clock is selected, and bLDO3V3_OFF=1, LDO is off, after complete sleep			0.008	0.02	mA
IADC5	ADC analog to digital conversion module working current			200	800	uA
ICMP5	Voltage comparator module working current			100	500	uA
ITKEY5	Touch key capacitance detection module working current			150	250	uA
VIL5	Low level input voltage		-0.4		1.2	V
VIH5	High level input voltage		2.4		VCC+0.4	V
VOL5	Low level output voltage (12mA draw current)				0.4	V
VOH5	High level output voltage (8mA output current)		VCC-0.4			V
VOH5U	P3.6/P3.7 high level output voltage (8mA output current)		V33-0.4			V

IIN	Input current of input terminal with no built-in pull-down resistor	-5	0	5	uA
IDN5	Input current of the input terminal with the built-in pull-down resistor	-35	-70	-140	uA
IUP5	Input current of the input terminal with the built-in pull-up resistor	35	70	140	uA
IUP5X	Input current of the input terminal with the built-in pull-up resistor during the turnover from low to high	250	400	600	uA
Vpot	Threshold voltage of power on reset of power supply	2.1	2.3	2.5	V

18.3 Electrical Parameters at 3.3V

Test Conditions: TA=25℃, VCC=V33=3.3V, Fsys=6MHz

Name	Parameter description		Min.	Typ.	Max.	Unit
VCC3	VCC pin supply voltage	V33 is short-connected to VCC, and turn on USB	3.0	3.3	3.6	V
		V33 is short-connected to VCC, and turn off USB	2.7	3.3	3.6	V
ICC16M3	Total supply current during operation at Fsys=16MHz		4	6		mA
ICC6M3	Total supply current during operation at Fsys=6MHz		2	4		mA
ICC750K3	Total supply current during operation at Fsys=750KHz		1	2		mA
ISLP3	Total supply current after sleep			0.07	0.15	mA
ISLP3L	Total supply current when bLDO3V3_OFF=1 and LDO is off, after complete sleep			0.004	0.01	mA
IADC3	ADC analog to digital conversion module working current			150	500	uA
ICMP3	Voltage comparator module working current			70	300	uA
ITKEY3	Touch key capacitance detection module working current			130	200	uA
VIL3	Low level input voltage		-0.4		0.8	V
VIH3	High level input voltage		1.9		VCC+0.4	V
VOL3	Low level output voltage (8mA draw current)				0.4	V
VOH3	High level output voltage (5mA output current)		VCC-0.4			V
VOH3U	P3.6/P3.7 high level output voltage (8mA output current)		V33-0.4			V
IIN	Input current of input terminal with no built-in pull-down resistor		-5	0	5	uA
IDN3	Input current of the input terminal with the built-in pull-down resistor		-15	-30	-60	uA

IUP3	Input current of the input terminal with the built-in pull-up resistor	15	30	60	uA
IUP3X	Input current of the input terminal with the built-in pull-up resistor during the turnover from low to high	100	170	250	uA
Vpot	Threshold voltage of power on reset of power supply	2.1	2.3	2.5	V

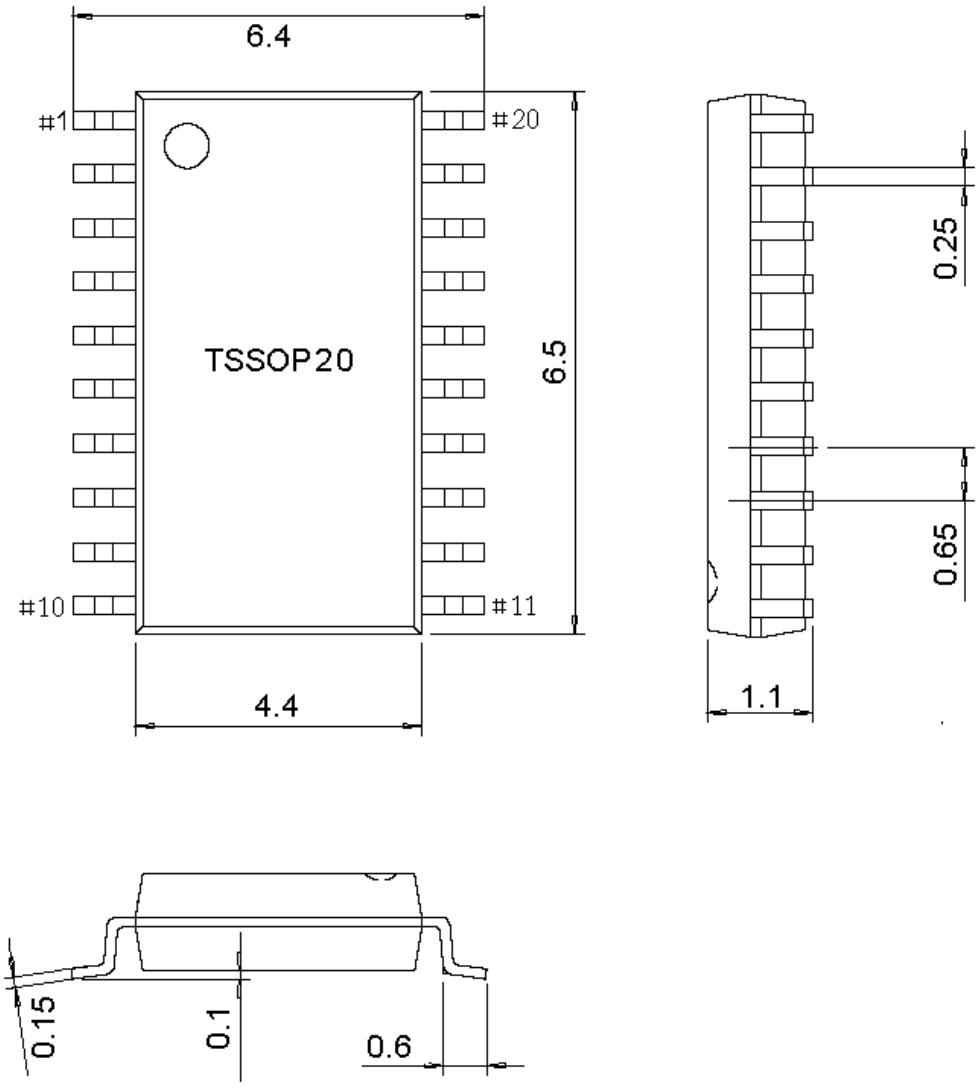
18.4 Timing Parameters

Test Conditions: TA=25℃, VCC=5V or VCC=V33=3.3V, Fsys=6MHz

Name	Parameter description	Min.	Typ.	Max.	Unit
Fxt	External crystal frequency or XI input clock frequency	6	24	25	MHz
Fosc	When V33=3V ~ 3.6V, the internal clock frequency after calibration	23.64	24	24.36	MHz
Fosc28	When V33=2.8V~3V, the internal clock frequency after calibration	23.28	24	24.72	MHz
Fosc27	When V33=2.7V, the internal clock frequency after calibration	21	24	25	MHz
Fpll	PLL frequency after internal frequency muitiplication	24	96	100	MHz
Fusb4x	USB sampling clock frequency when using USB device function	47.04	48	48.96	MHz
Fsys	System dominant frequency clock frequency (VCC>=4.4V)	0.1	6	24	MHz
	System dominant frequency clock frequency (4.4V>VCC>=3.3V)	0.1	6	16	MHz
	System dominant frequency clock frequency (VCC<3.3V)	0.1	6	12	MHz
Tpor	Power on reset delay of power supply	9	11	15	mS
Trst	Width of the input effective reset signal from the outside of RST	70			nS
Trdl	Thermal reset delay	30	45	60	uS
Twdc	Formula for watchdog overflow cycle/timing cycle	65536 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	Time to detect automatic USB suspension	4	5	6	mS
Twak	Wake-up completion time after chip sleep	1	2	10	uS

19. Package

19.1 TSSOP20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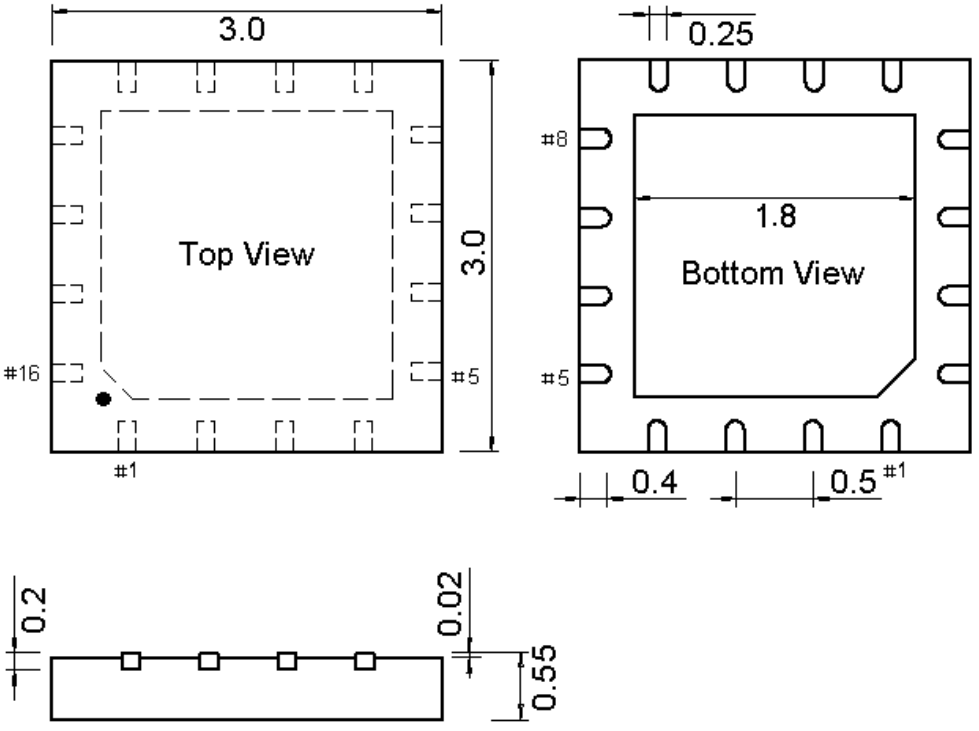
19.2 QFN16-3*3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3.0
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#5
#1
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#8
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0.2
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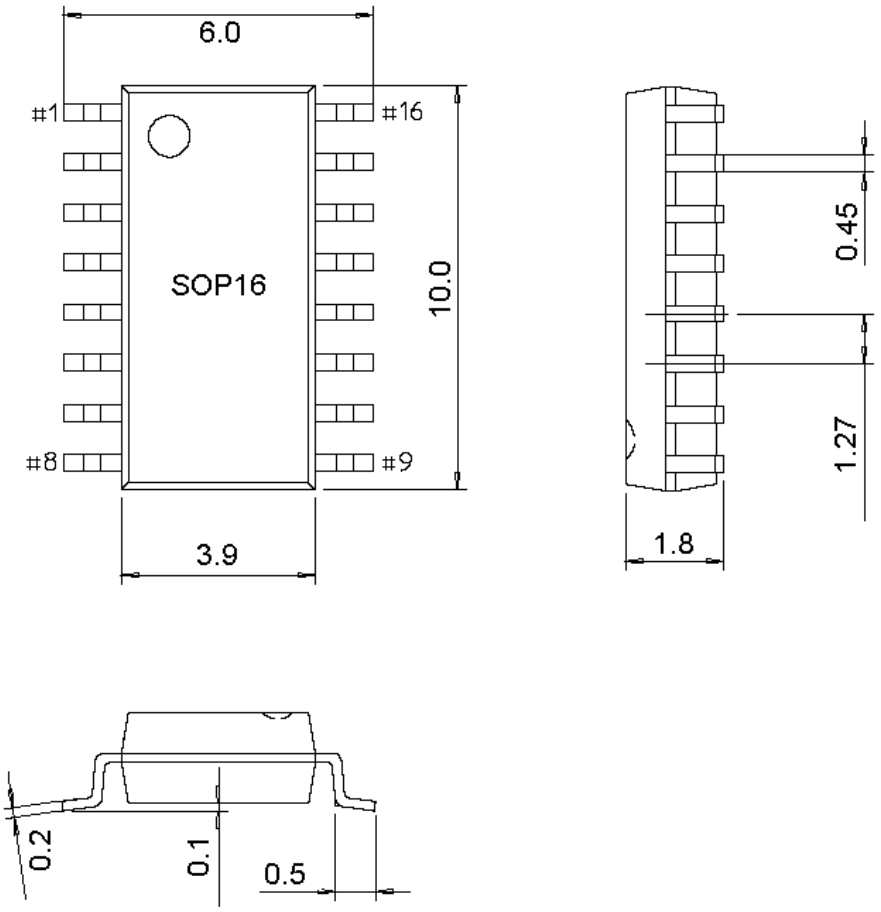
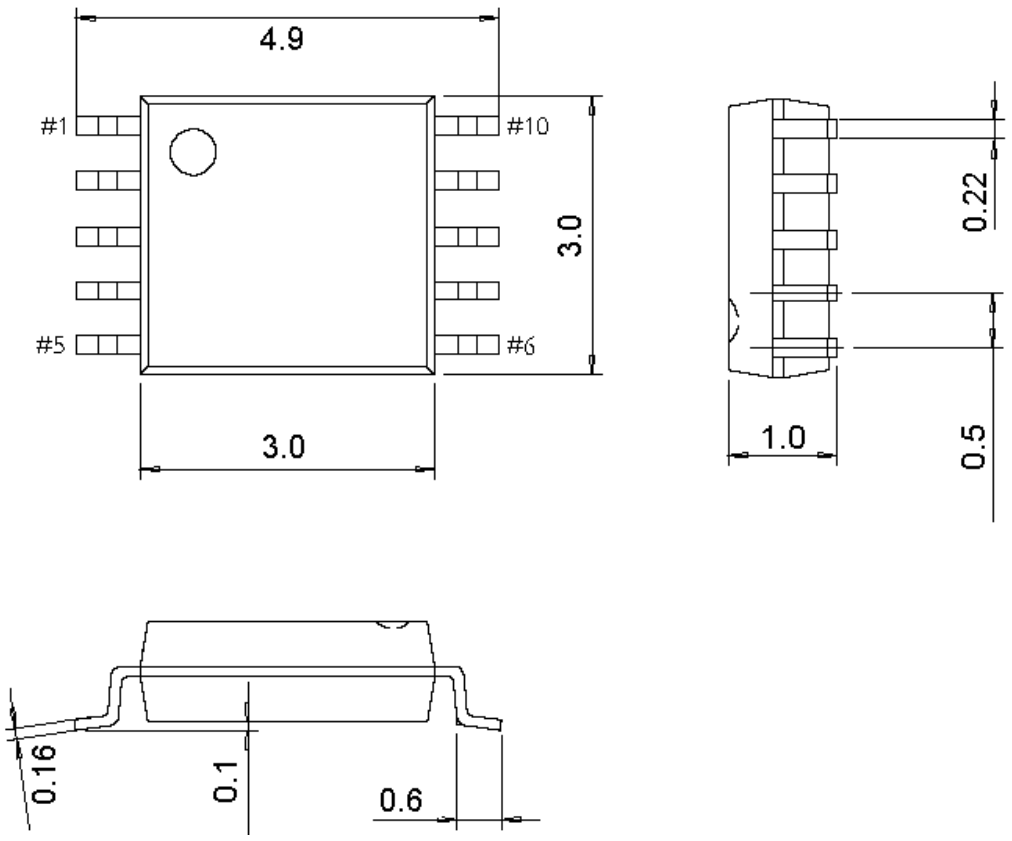
19.3 SOP16-150mil



19.4 MSOP10



20. Revision History

Version	Date,	Description
V1.0	December 20, 2016	First release
V1.1	September 12, 2017	The maximum dominant frequency of the system is adjusted to 24MHz, and section 8.2 and section 18.4 are updated
V1.2	December 16, 2017	Add the CH552/CH551 difference table to the overview and modify some header forms
V1.3	March 20, 2018	Modify the form of the CH552/1 difference table in 1. Overview and modify Table 18.4, Modify the wrongly written characters in section 5.3 Stack Pointer (SP), and add Data Flash suggestions in section 6.2
V1.4	August 28, 2018	Updated Fosc27 in section 18.4
V1.5	June 17, 2019	Add QFN16 package, update section 3,4, and add Chapter 19 Package